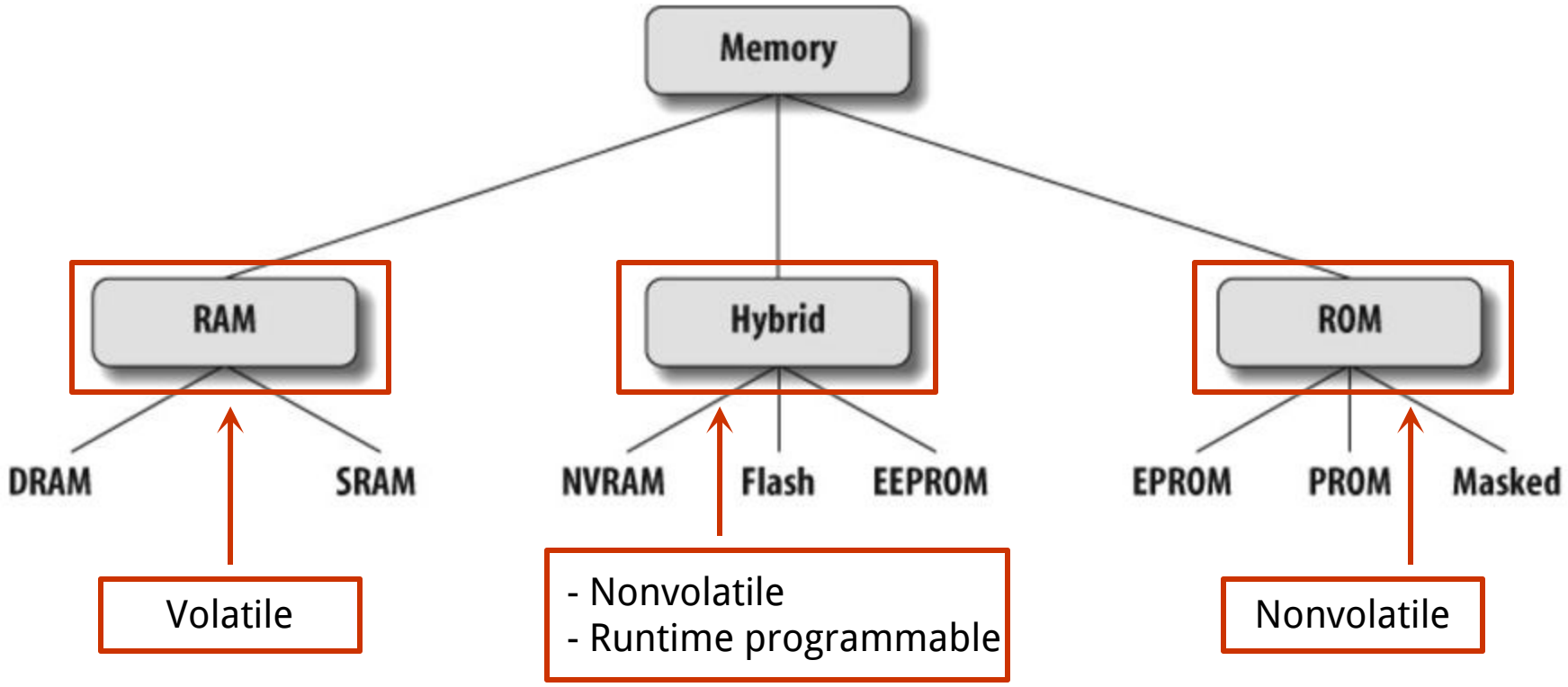
Microprocessors, Lecture 5

Memory Interfacing

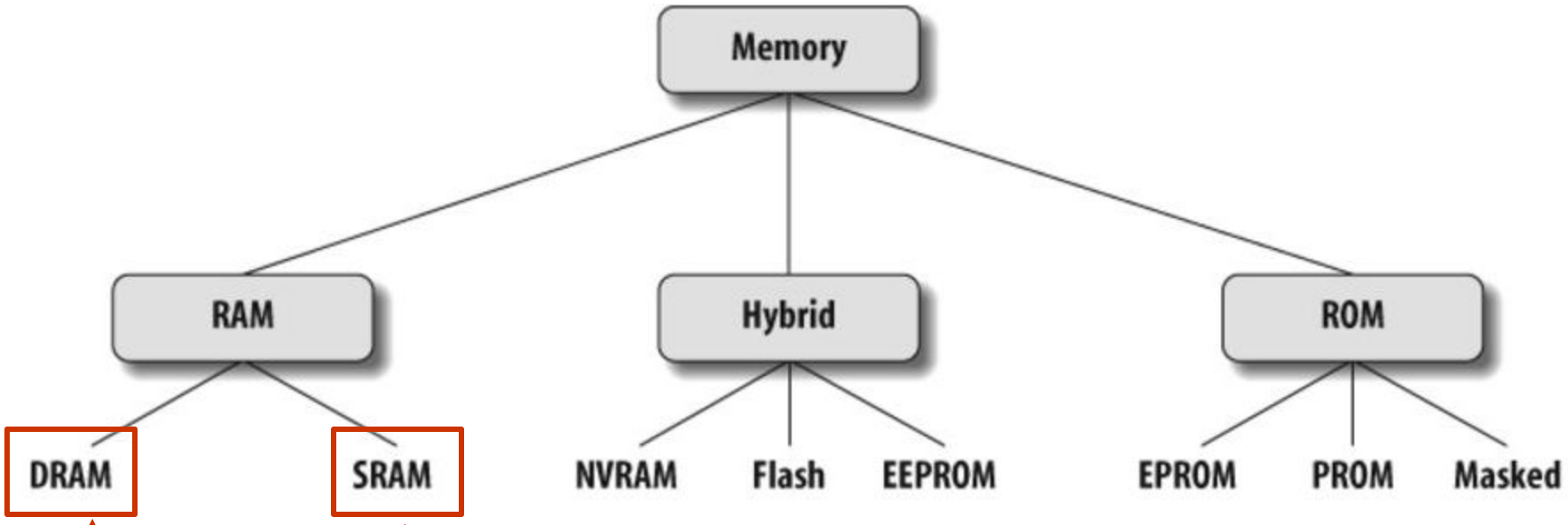
Hamid Fadishei
Assistant Professor, University of Bojnord
Spring 2015

Types of Memory



Volatile: loss of power => loss of data

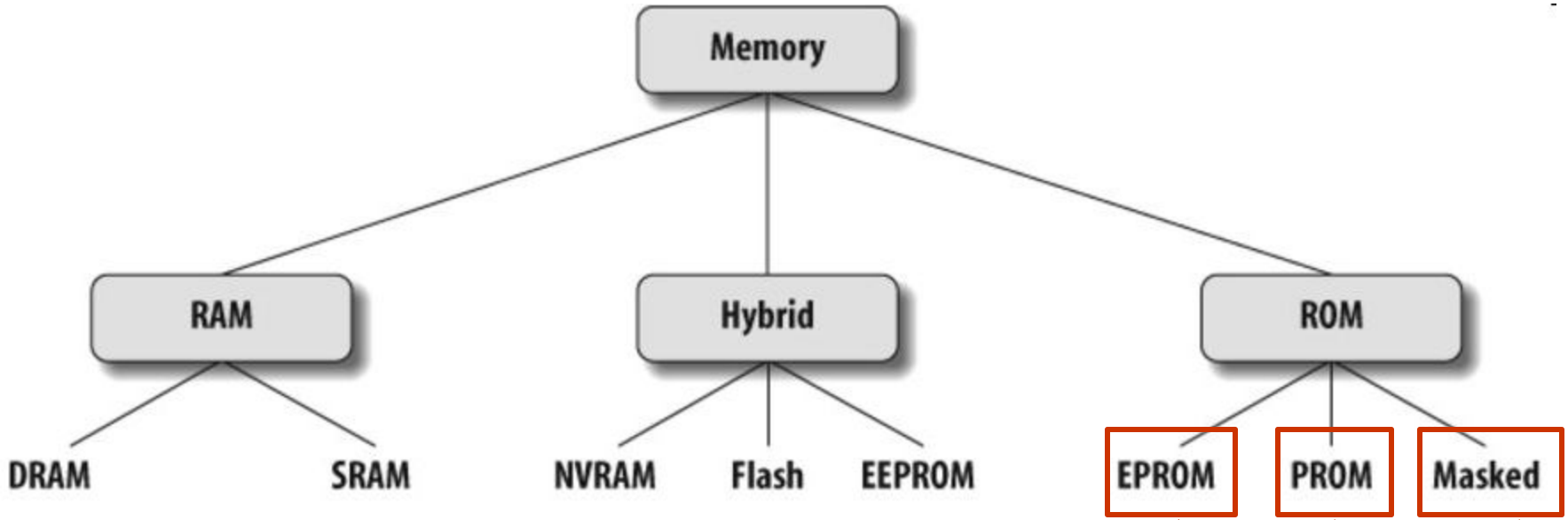
Types of Memory



- Static RAM
- Storage element is similar to FFs
- Faster compared to DRAM

- Dynamic RAM
- Storage is based on capacitance charge
- Needs to be refreshed periodically
- Cheaper (less transistors) compared to SRAM

Types of Memory



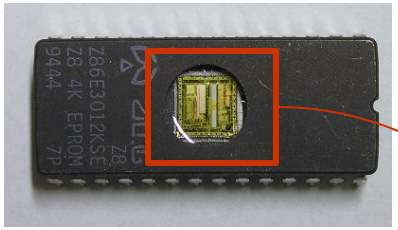
- Electrically programmable
- Erasable by ultraviolet light

- Programmable ROM
- Programmed by burning fuses inside
- Not erasable

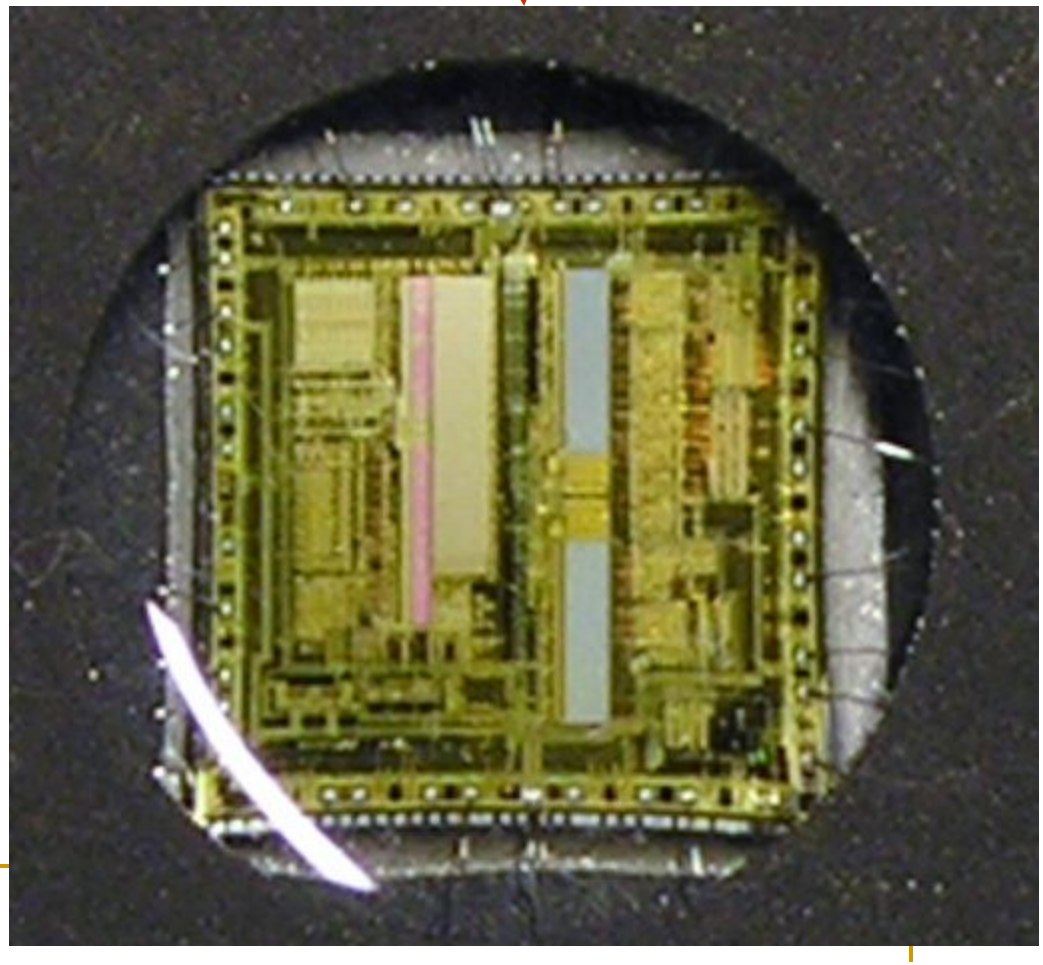
- Programmed at manufacturing
- Not erasable

EPROM

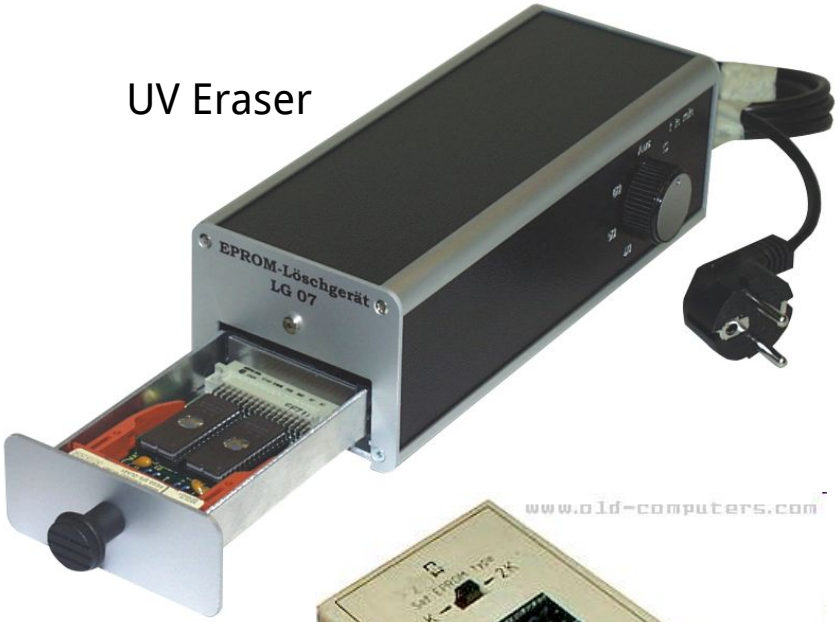
Almost obsolete today!

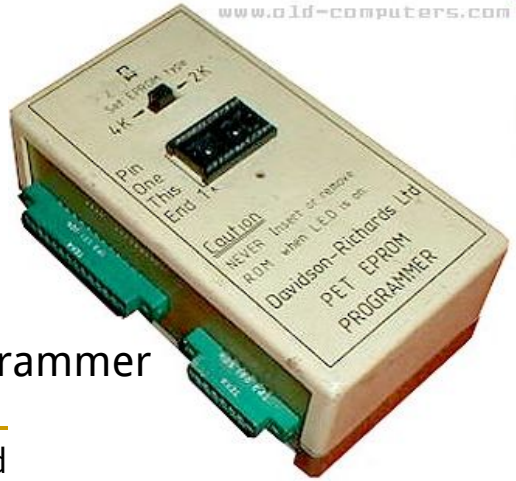


EPROM



UV Eraser

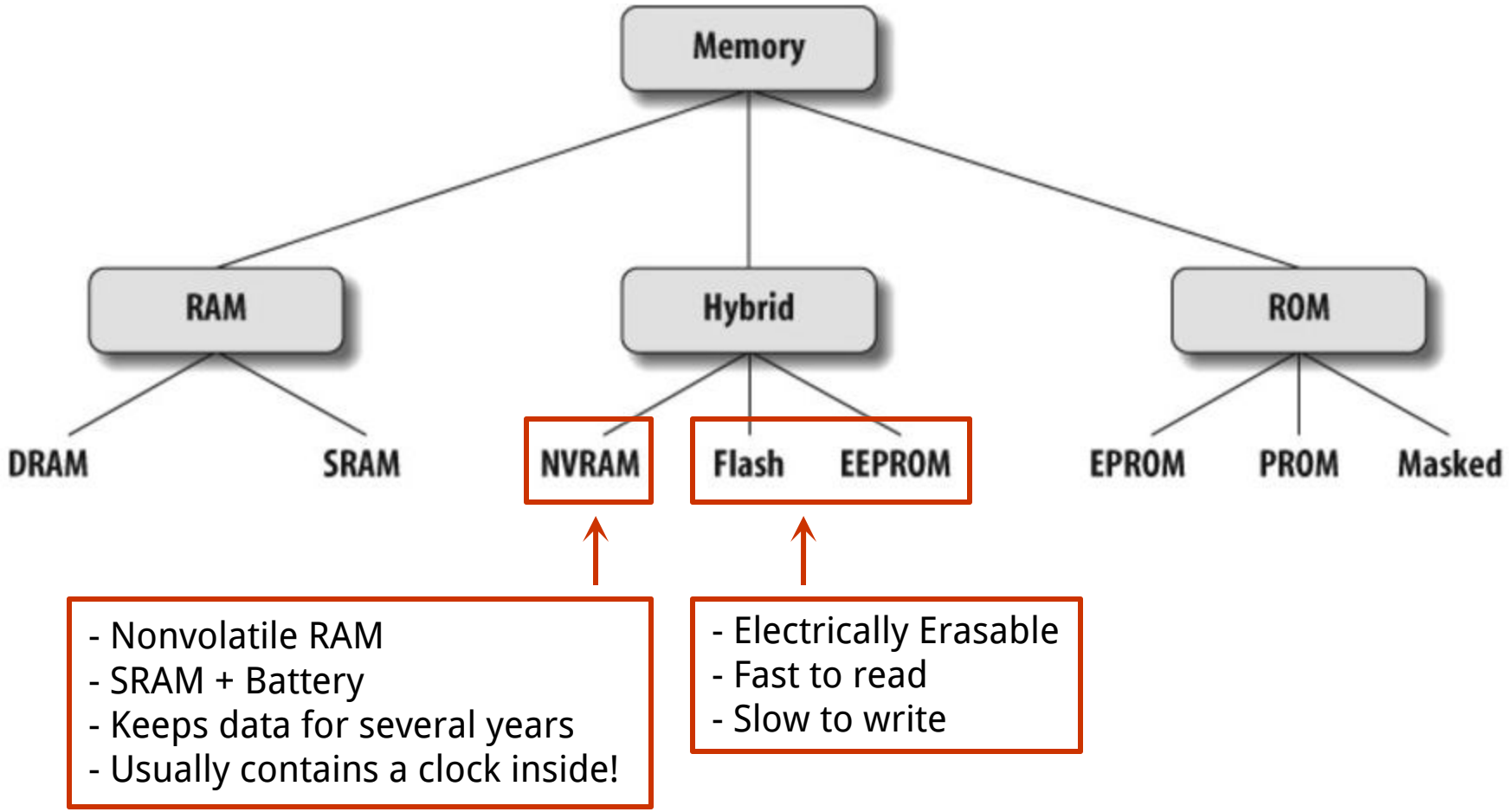


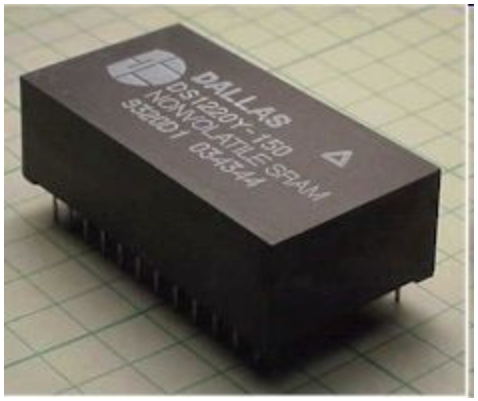


EPROM Programmer

Hamid Fad
University of Bojnord

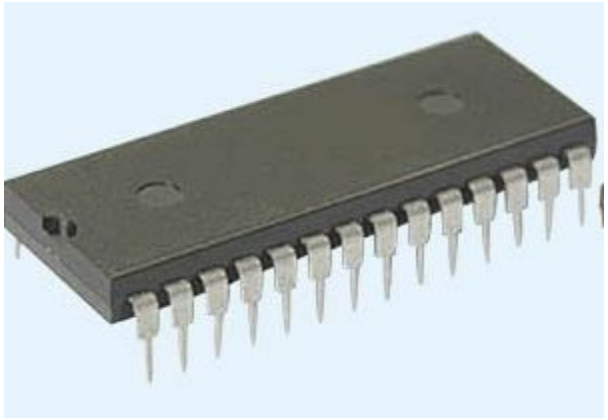
Types of Memory





NVRAM

Flash



EEPROM

Serial EEPROM

Universal Programmer

Memory interfacing

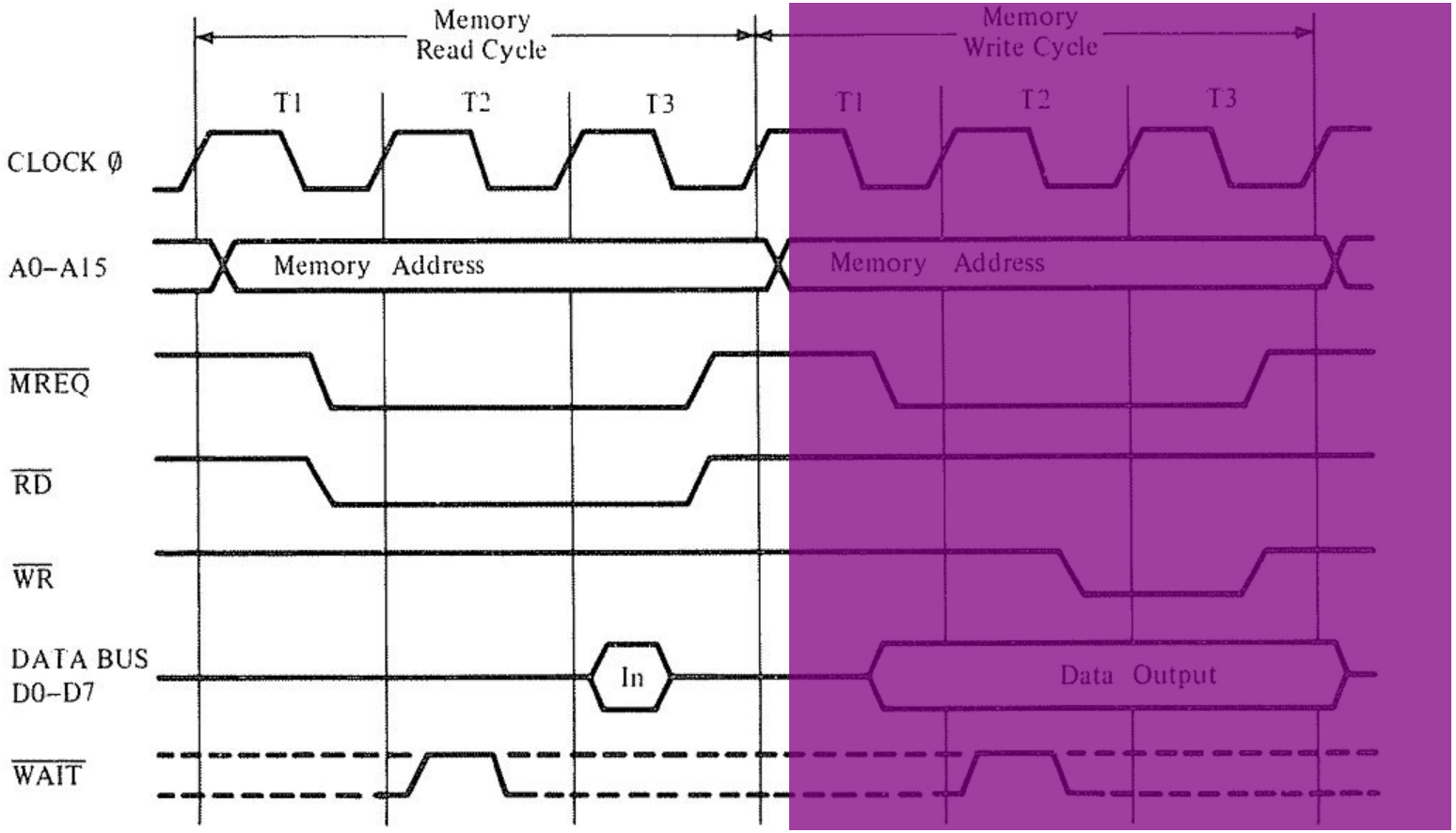
- Question: How to interface a (Z80) microprocessor to a memory chip?
  - We should first answer these two questions:
    - How does Z80 works with memory?
    - How does the memory chip expect to be worked with?
- The requirements that should match
  - Timing
  - Electrical characteristics
  - Data format

Z80 Side

- How does Z80 work with memory?
  - Z80 memory operations
    - Read
      - Places a 16 bit address on its address bar
      - Asserts MREQ to indicate address bus holds a valid address
      - Asserts RD to indicate that it wants to read
    - Write
      - Places a 16 bit address on its address bar
      - Asserts MREQ and places data on its data bus
      - Asserts WR signal

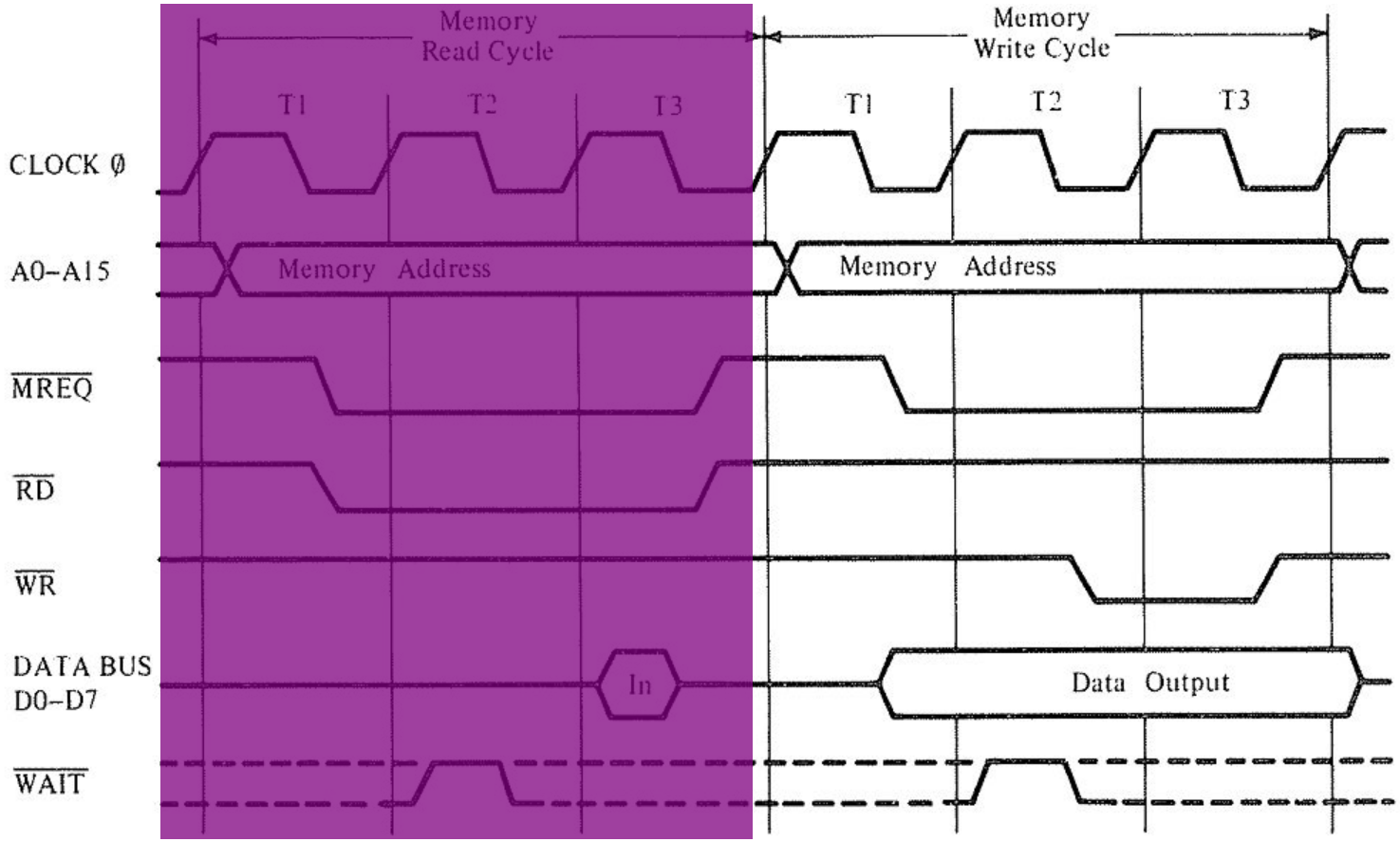
Z80 Side

- Z80 memory read timing



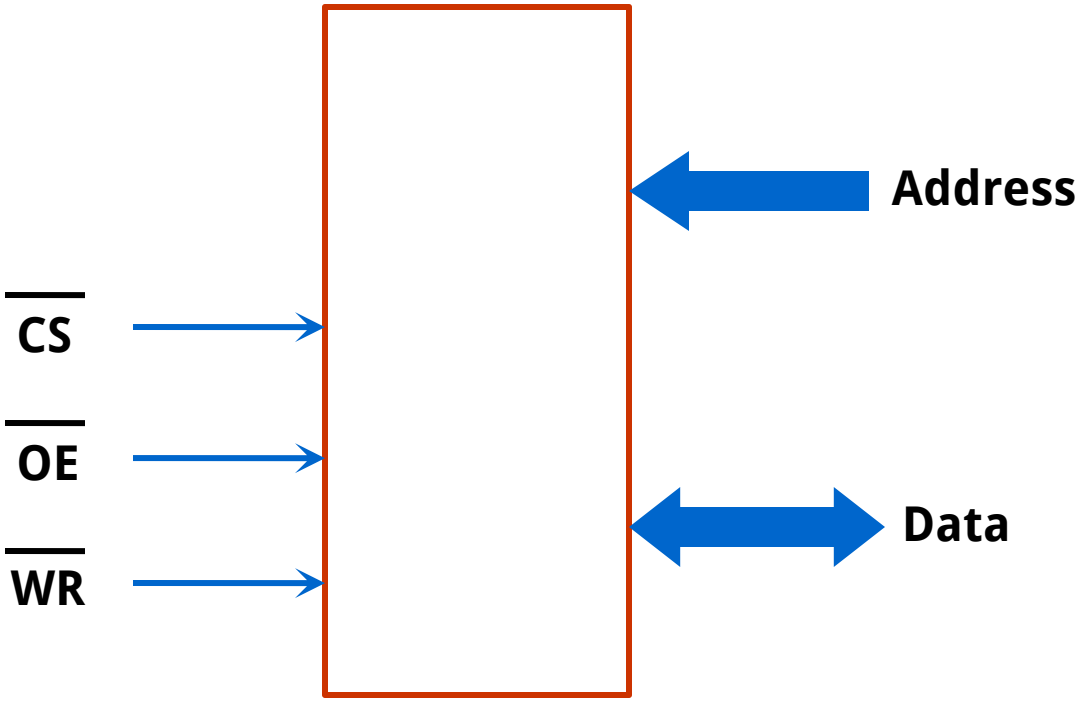
Z80 Side

- Z80 memory write timing



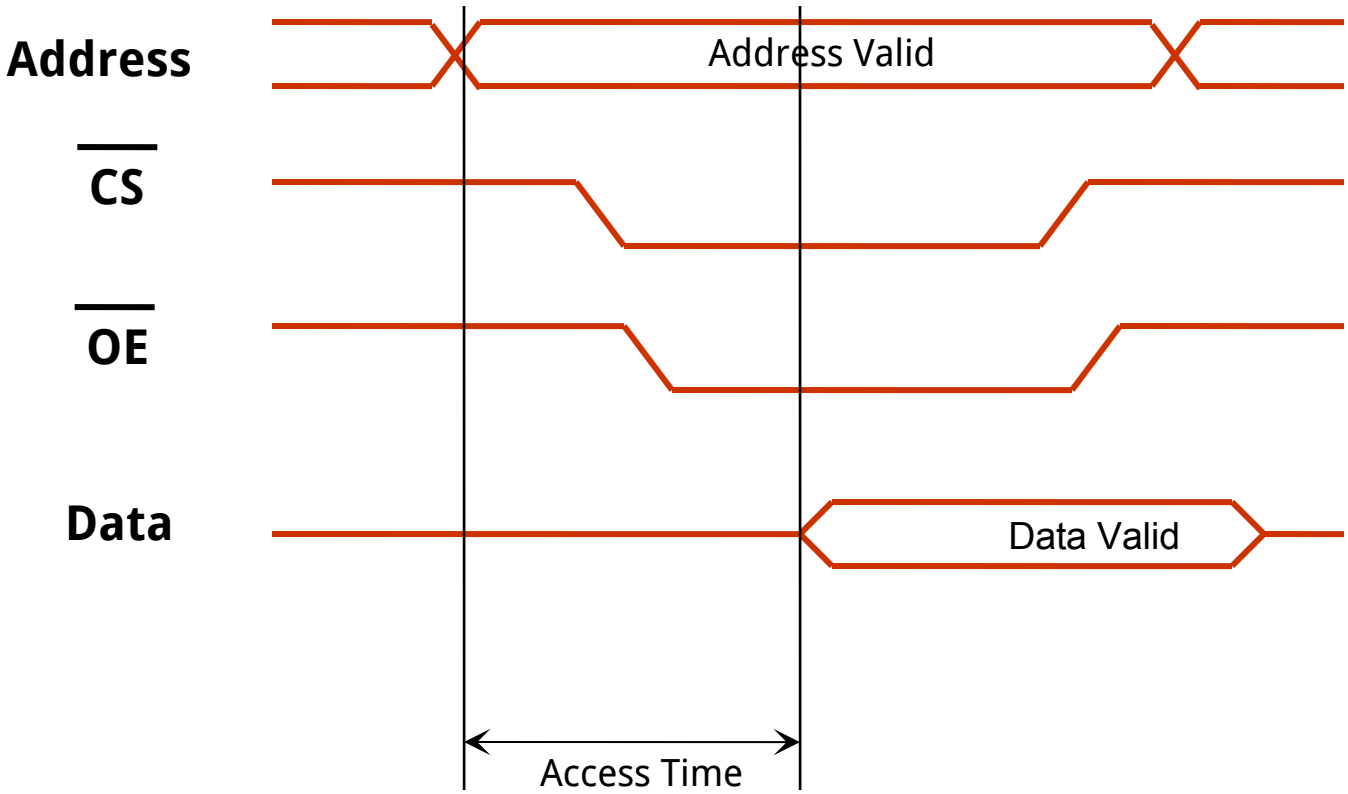
Memory side

- Typical memory unit
  - Address pins
  - Data pins
  - Control pins
    - Chip select
    - Output enable
    - Write



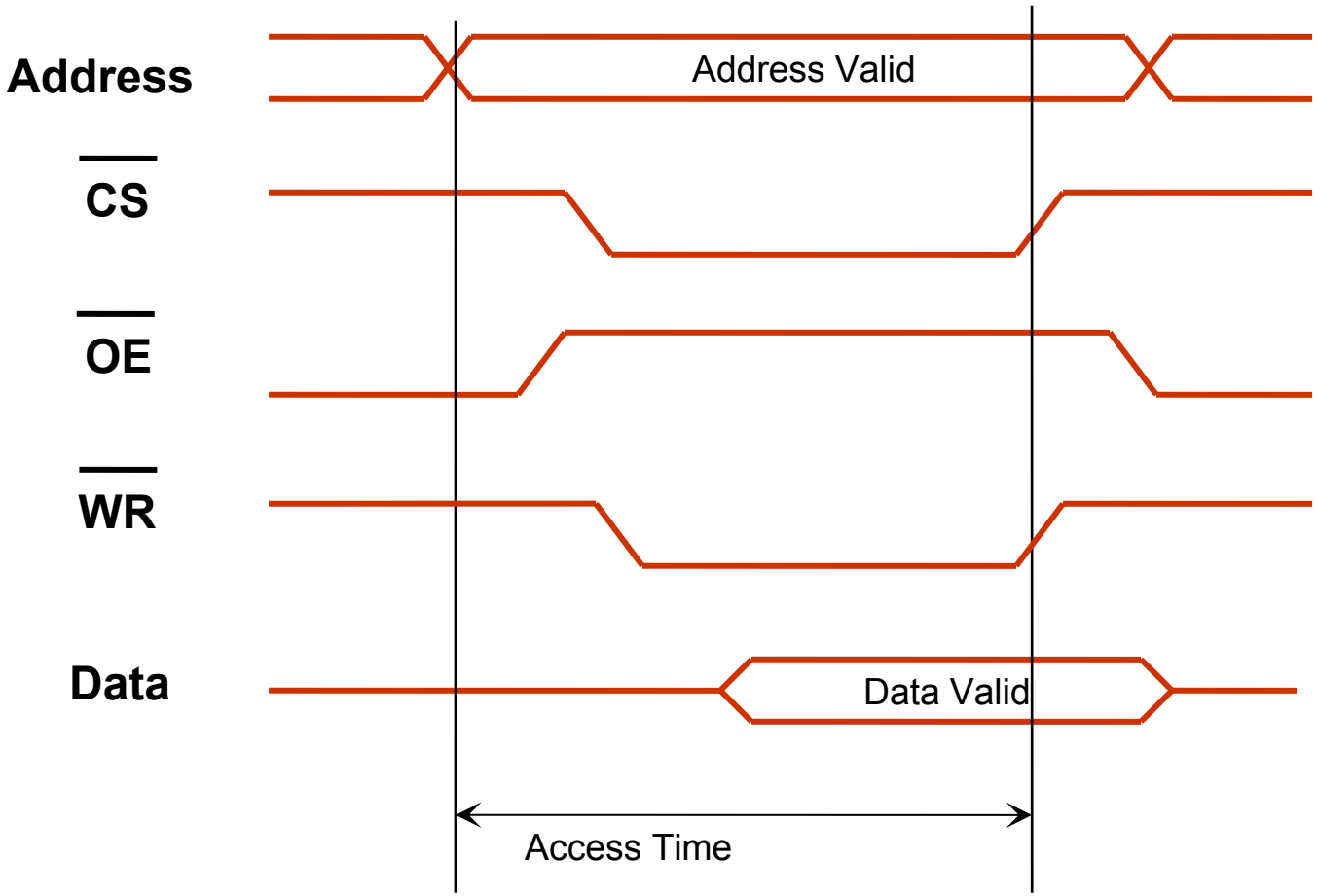
Memory Side

- Memory read timing



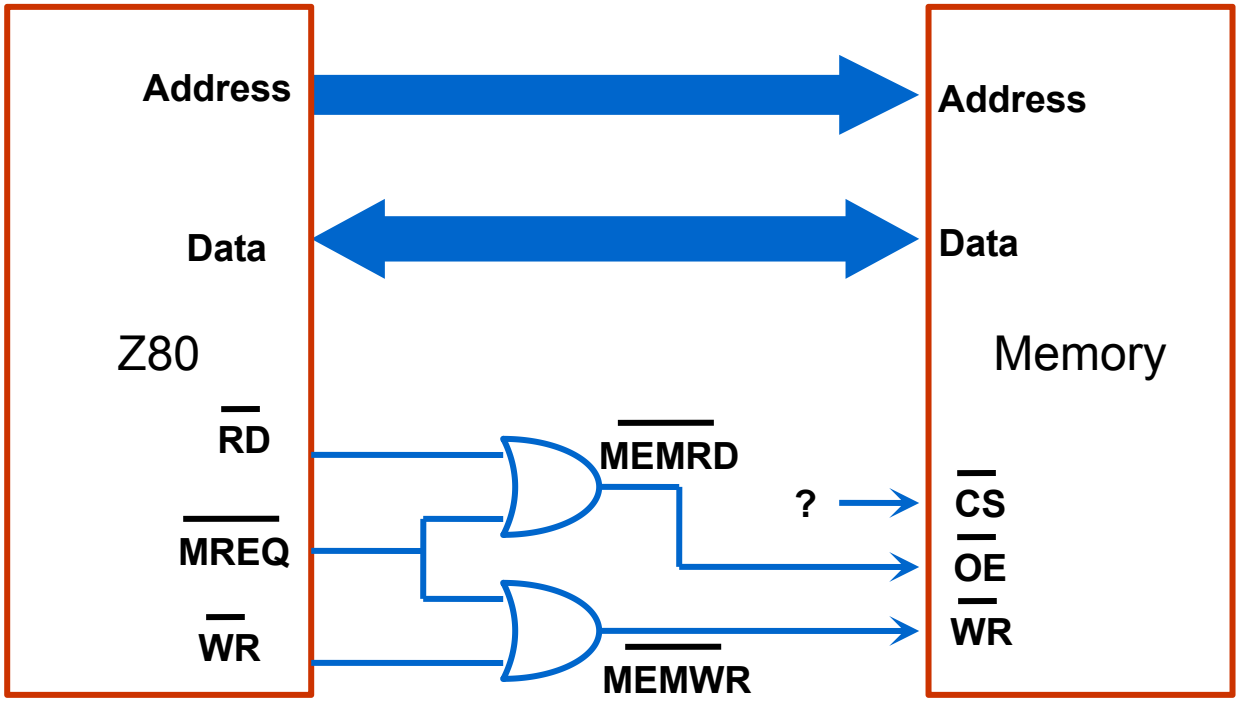
Memory Side

- Memory write timing



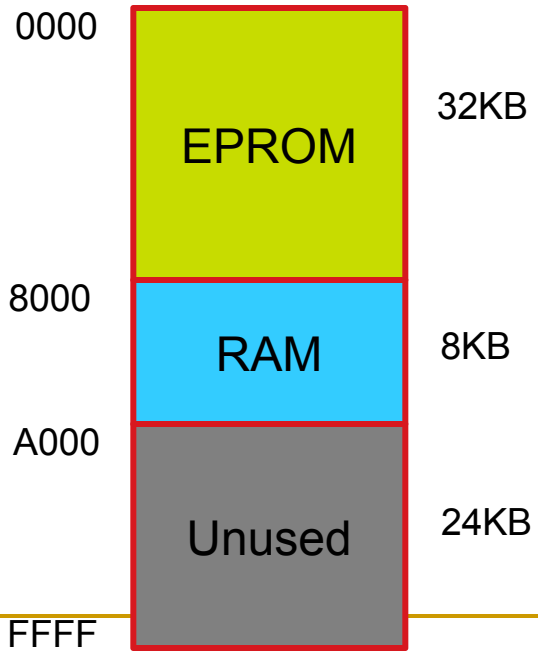
Z80 – Memory interconnection

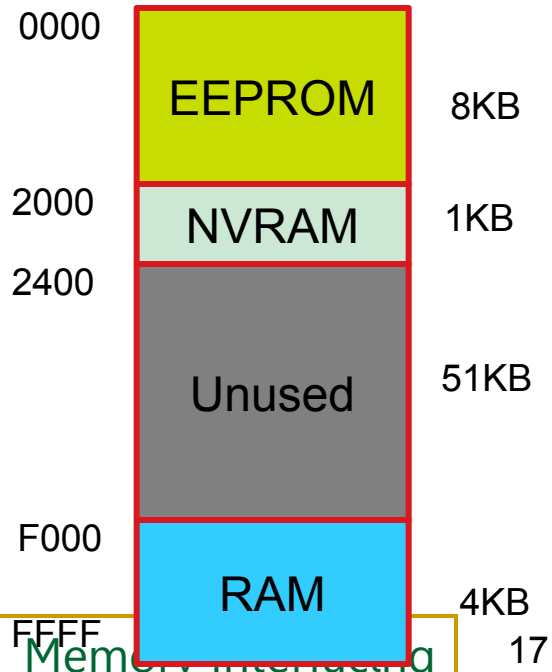
- Interfacing memory to Z80



Memory Mapping

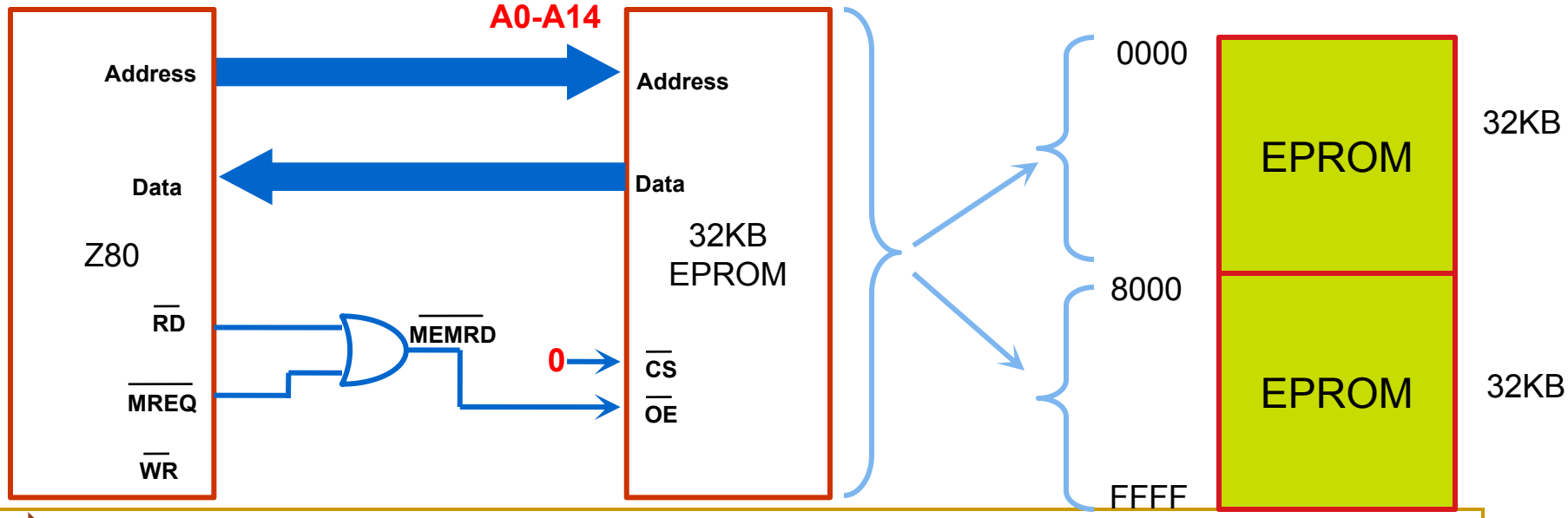
- Address space
  - The set of all addresses that can be accessed by a microprocessor
- Address space partitioning
  - A microprocessor is generally interfaced to several memory chips
  - Address space should be partitioned into subsets
  - Each chip should be mapped to a subset (address mapping)
- Examples



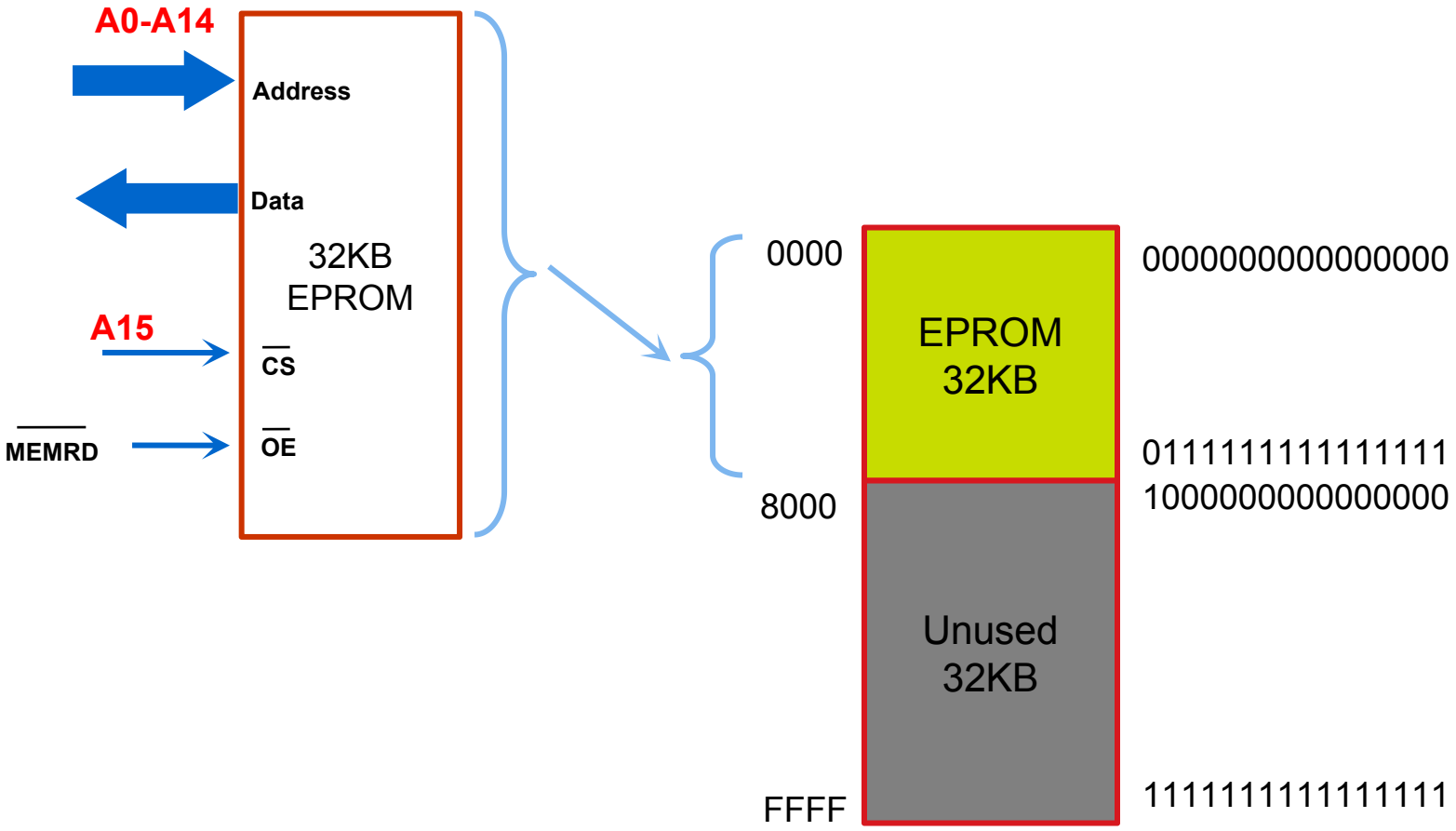


Memory Mapping

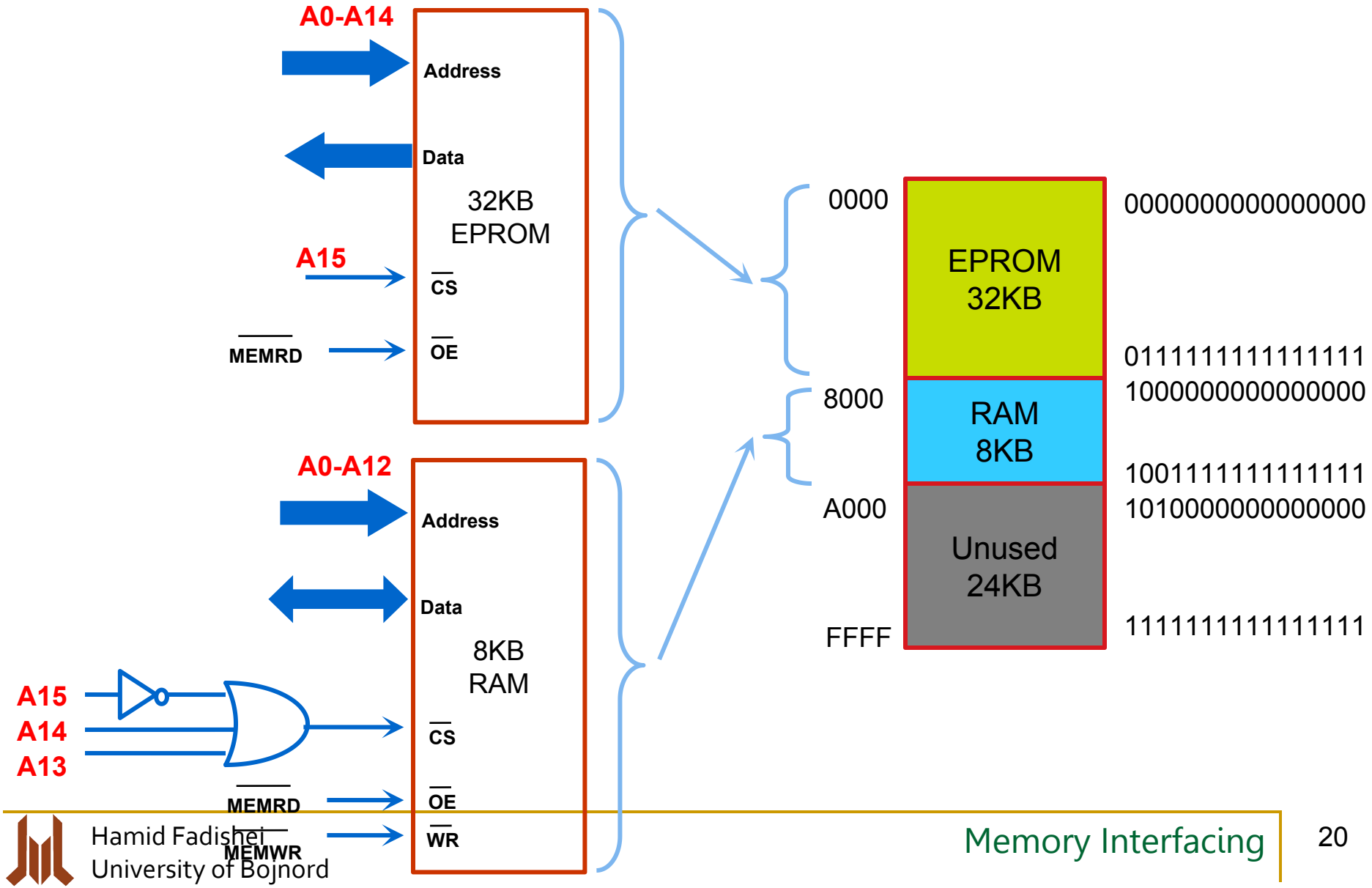
- Let's always keep the chip selected
  - Memory chip is mapped multiple times
  - An address decoder eliminates this behavior
    - Input: high order bits of address
    - Output: Chip-select signals
  - May be ignored if we need simpler designs



Memory Mapping

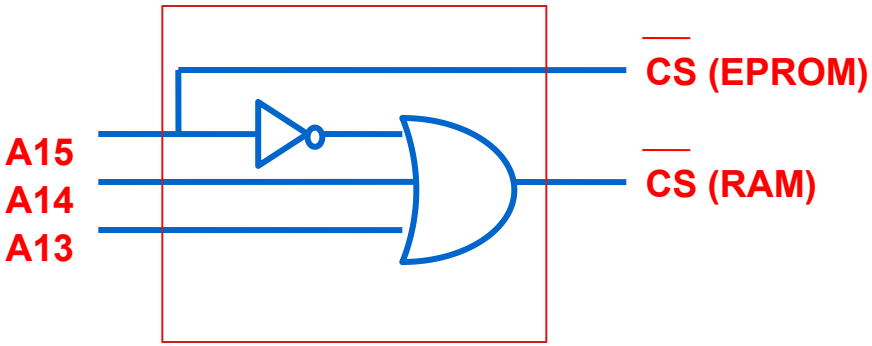


Memory Mapping



Memory Mapping

- Address decoder

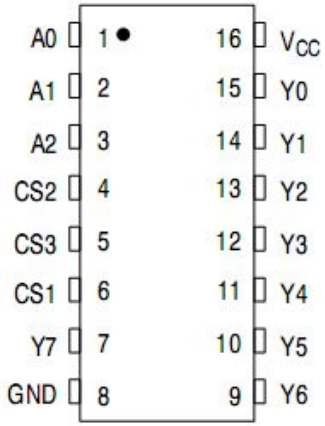


Some part numbers

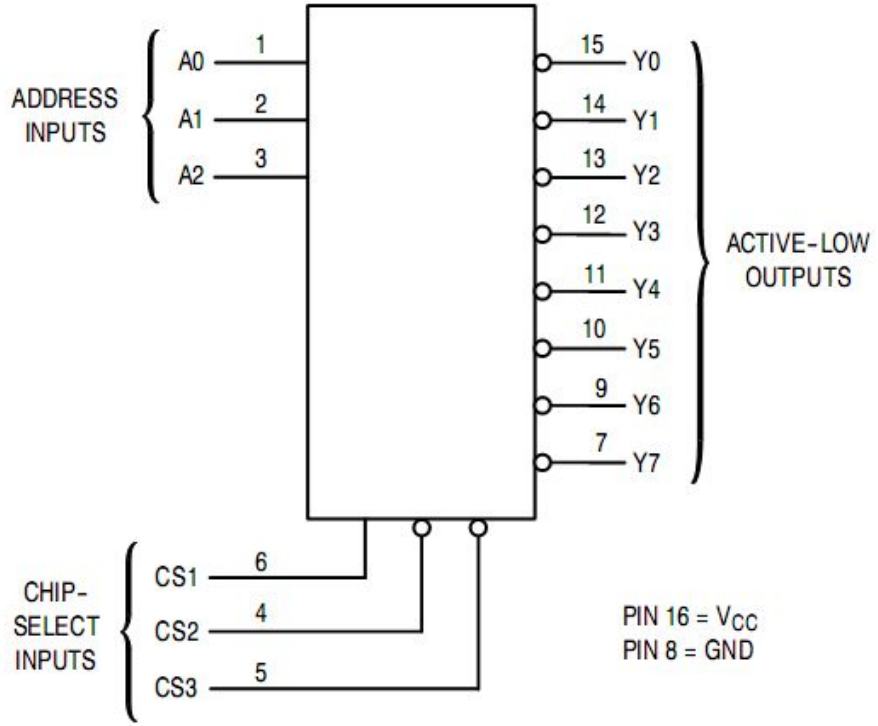
- SRAM
  - 6116
    - 16 Kbits (2KBytes) static RAM
- EPROM
  - 2764
    - 64 Kbits (8KBytes) EPROM
- EEPROM
  - AT28C256
    - 256 Kbits (64KBytes) EEPROM
- NVRAM
  - M48Z02
  - 2KBytes NVRAM

Address decoding chips

- 74138 3-to-8 decoder

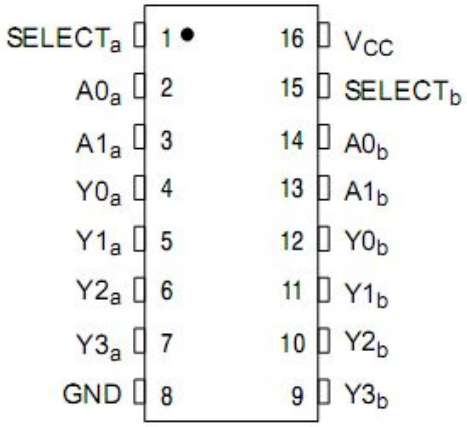


Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

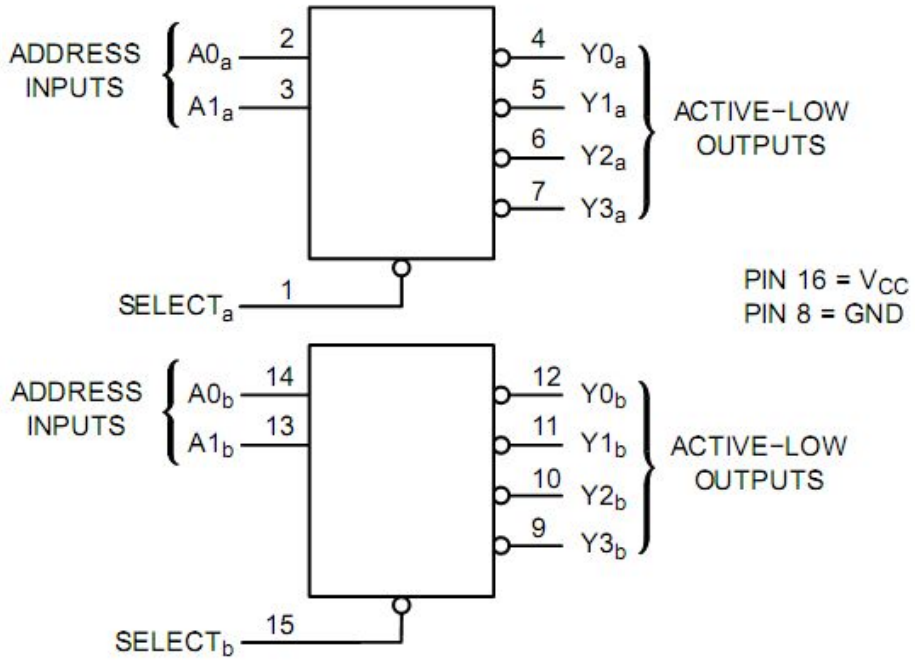


Address decoding chips

- 74139 dual 2-to-4 decoder

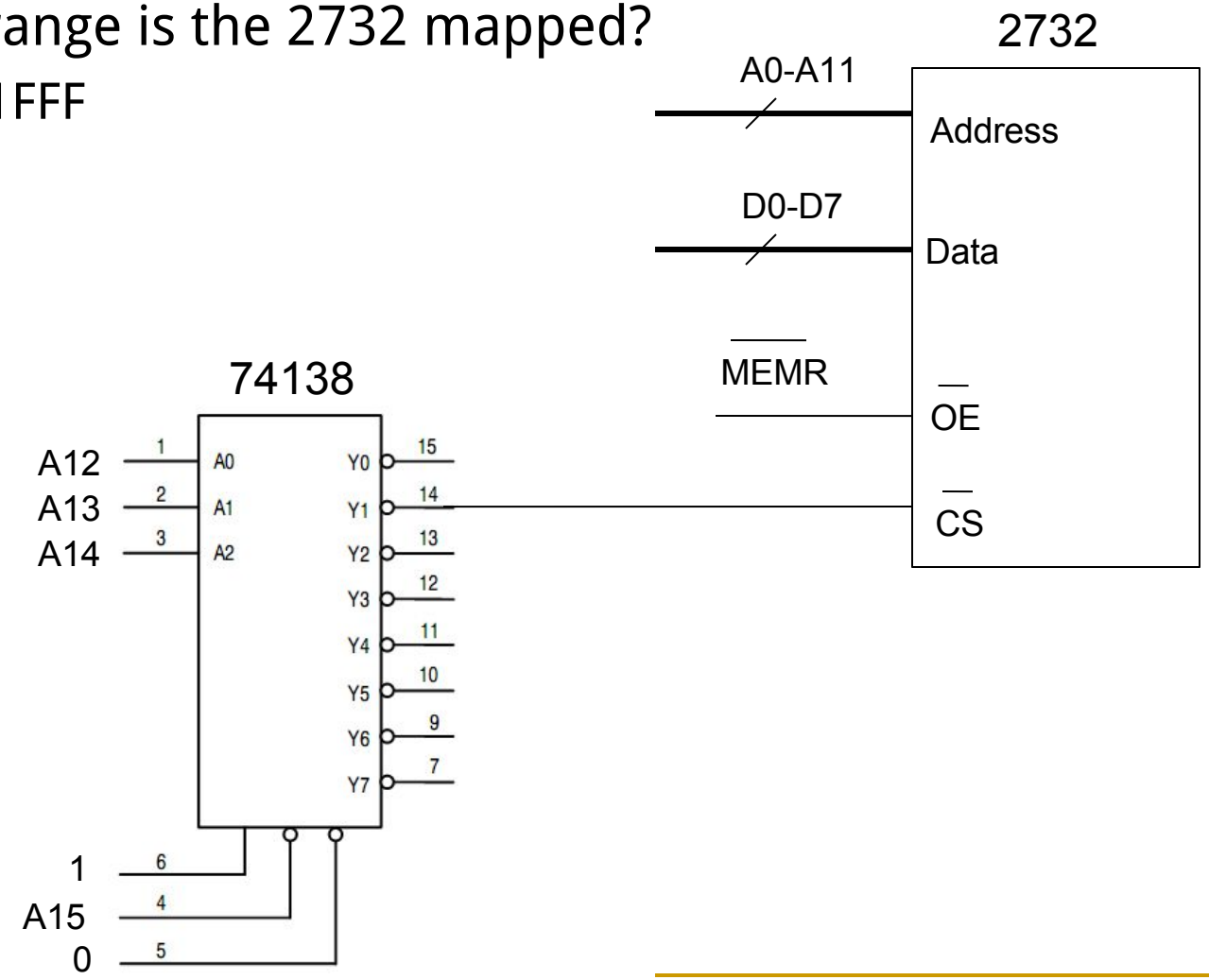


Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L



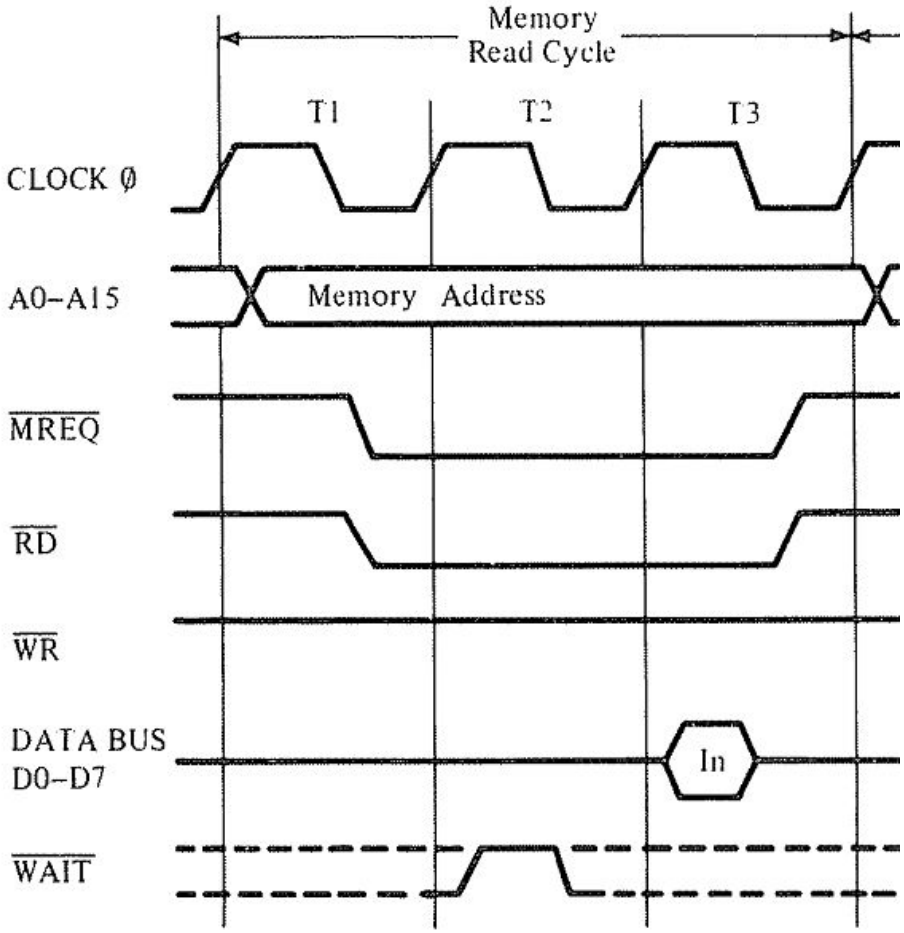
Address decoding chips

- Example usage
  - In what range is the 2732 mapped?
    - 1000-1FFF



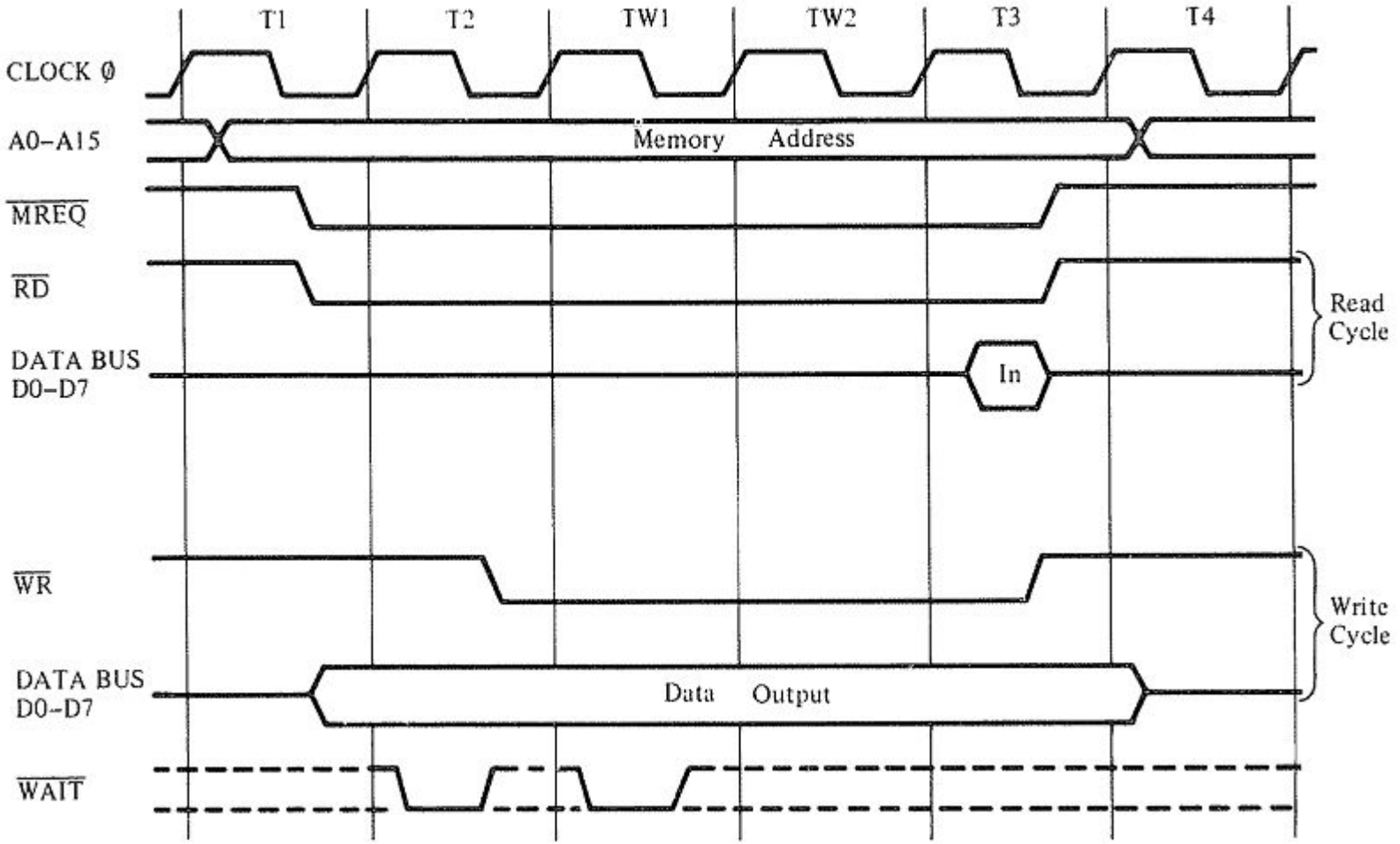
Slow memories

- Let's look again at Z80 memory timing
  - waits less than 2 clock cycles for memory
  - What if memory access time is longer?
- Adding wait states
  - You should assert WAIT in T2
  - Then Z80 will add a wait state Tw
  - You may keep WAIT active extra wait states



Slow memories

- Read/Write with wait states



Slow memories

- Adding one wait state to each memory cycle