Microprocessors, Lecture 2

The Z80 Microprocessor

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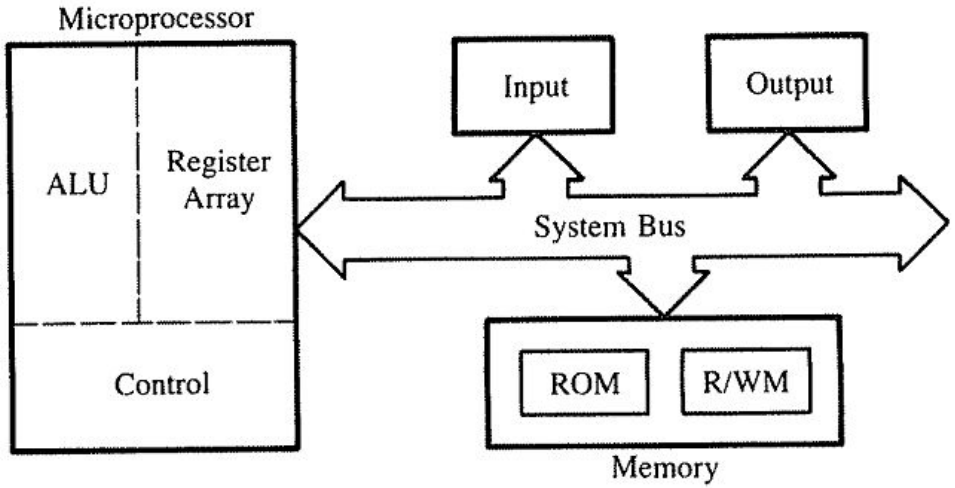
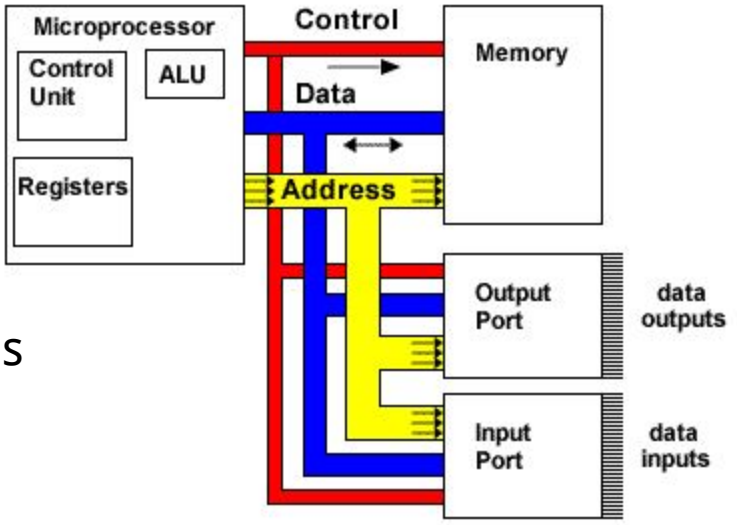
Microprocessor system

- What a µP does
  - Fetch some instructions from memory one-by-one
  - Decode the instruction
  - Execute the instruction
- Bus architecture
- µP-World Operations
  - Initiated by µP
    - Memory read
    - Memory write
    - I/O read
    - I/O write
- Initiated by external world
  - Reset
  - Interrupt
  - Wait (for slow memories)
  - Bus request (for DMA operation)



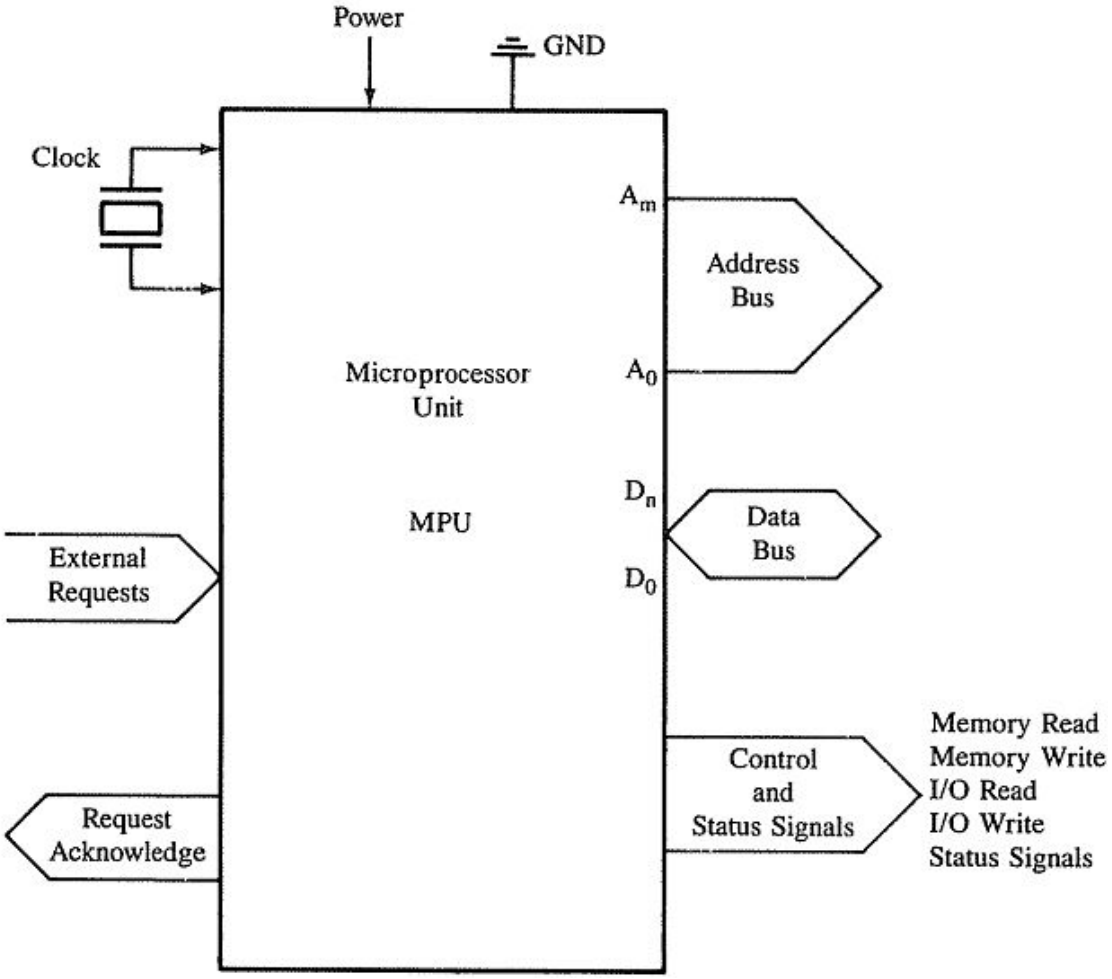
Bus architecture

- Bus architecture
  - Data bus
    - Binary data to write or read
  - Address bus
    - Memory addressing
      - Which memory chip
      - Which memory location
    - To identify Input/Output peripherals
      - Which peripheral
      - Which location
  - Control signals
    - Indicates µP operation
      - Memory/IO
      - Read/Write



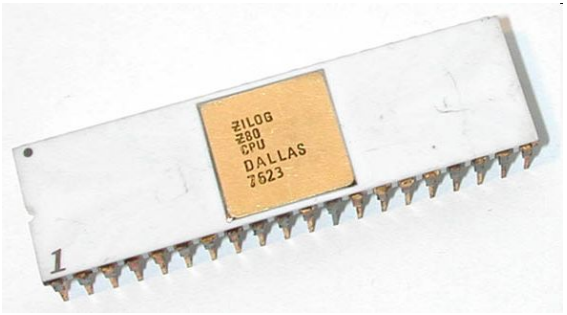
A Typical microprocessor

- So, a typical microprocessor looks like…



Zilog Z80

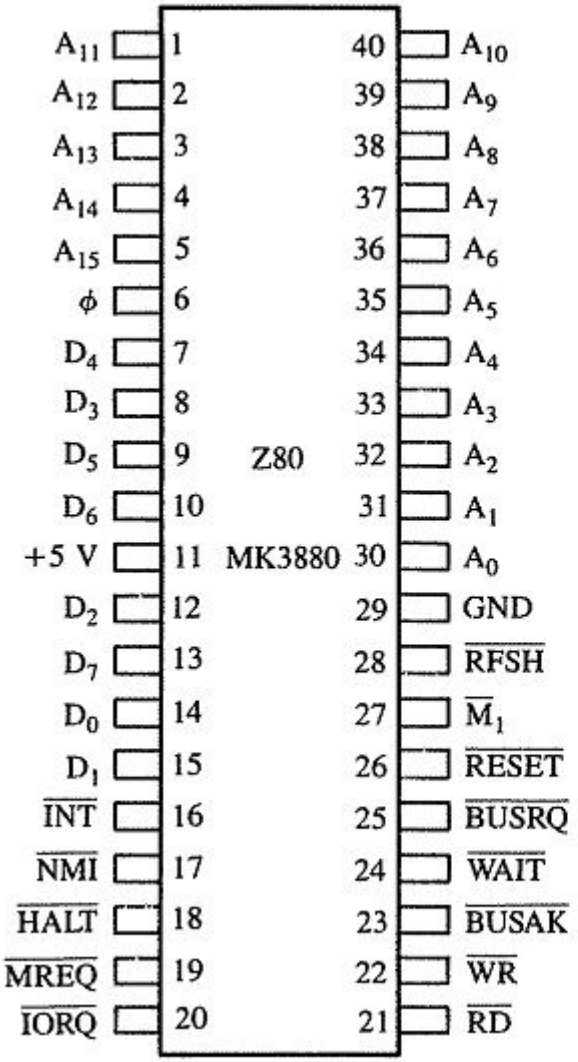
- Zilog Z80
  - An 8-bit microprocessor introduced in July 1976
  - Designed by Frederico Faggin after he left Intel
  - He was a main member of the team who designed 4004, 8008, and 8080
  - Z80 is one of the most popular microprocessor of all time
  - Many variants of this µP are still in use and manufactured by Zilog and other companies
  - Many µCs with a Z80 core are manufactures today

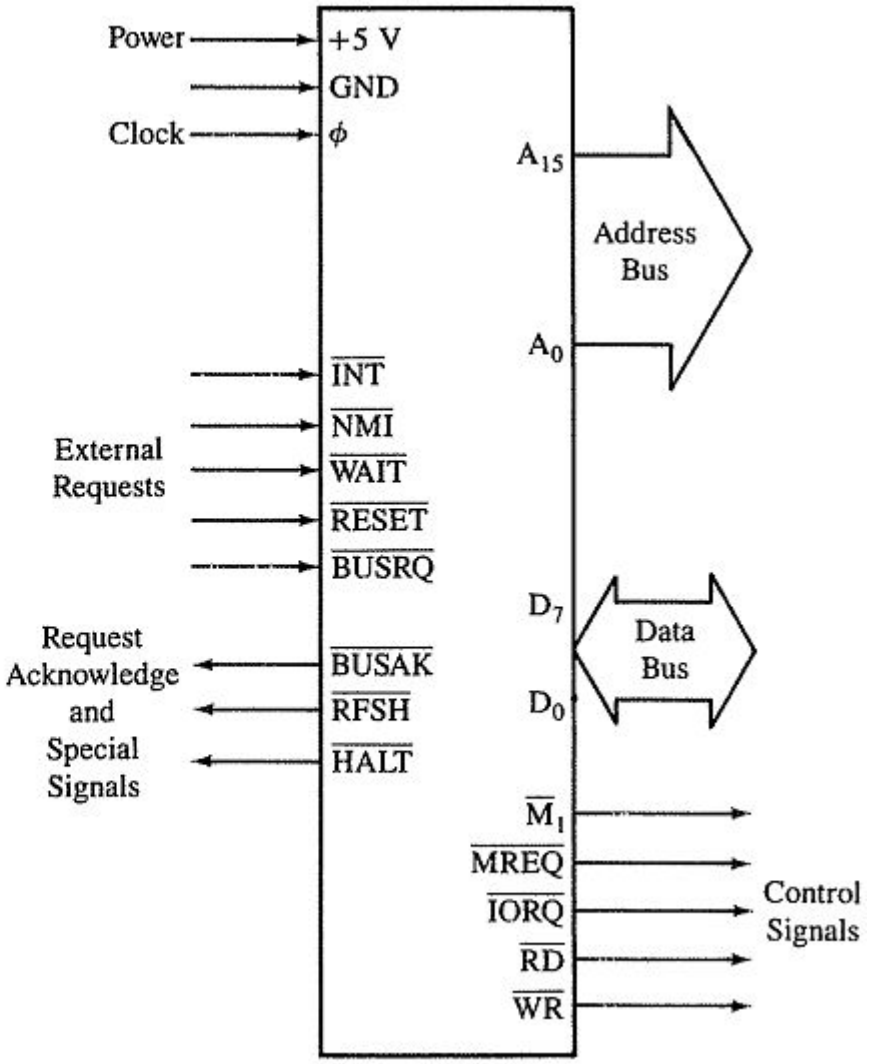


Original Z80 microprocessor running at 2.5Mhz

Z80180 feature-rich microcontroller running at up to 33Mhz

Z80 Pins

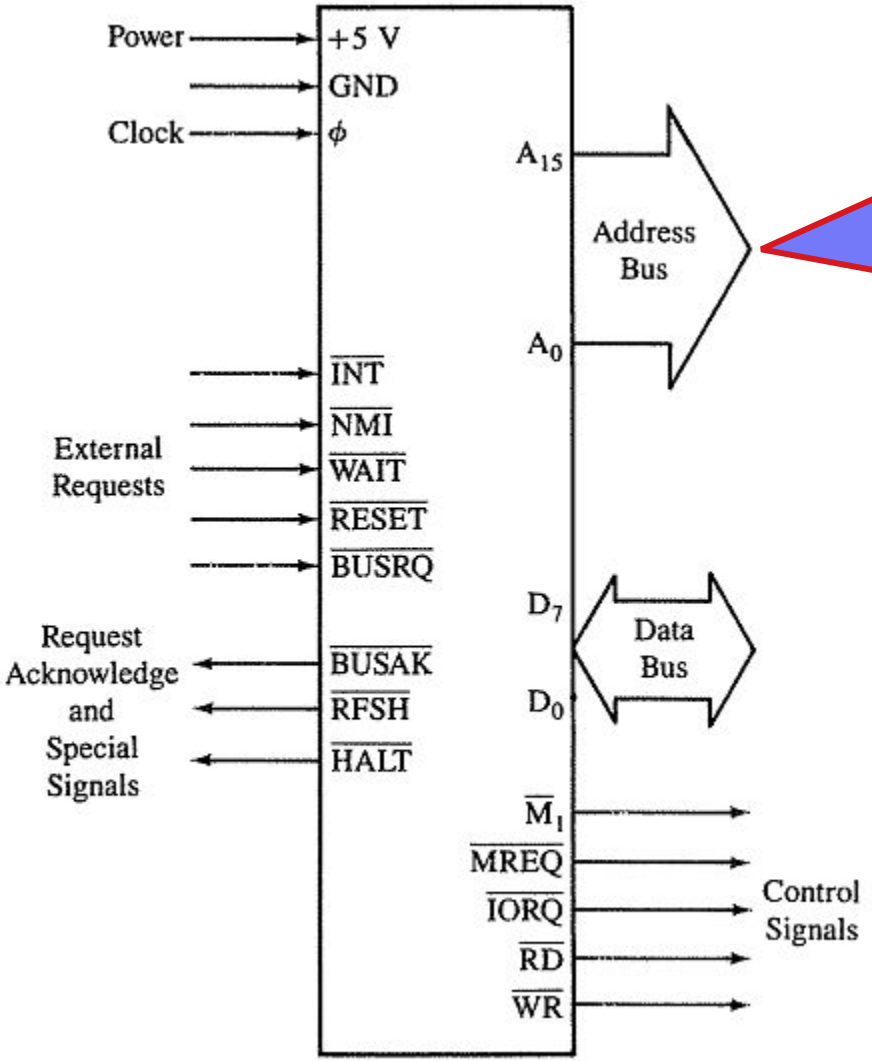

A11 1
A12 2
A13 3
A14 4
A15 5
φ 6
D4 7
D3 8
D5 9
D6 10
+5 V 11
D2 12
D7 13
D0 14
D1 15
INT 16
NMI 17
HALT 18
MREQ 19
IORQ 20
Z80
MK3880
40 A10
39 A9
38 A8
37 A7
36 A6
35 A5
34 A4
33 A3
32 A2
31 A1
30 A0
29 GND
28 RFSH
27 M1
26 RESET
25 BUSRQ
24 WAIT
23 BUSAK
22 WR
21 RD


Power
Clock
+5 V
GND
φ
A15
Address Bus
A0
INT
NMI
WAIT
RESET
BUSRQ
External Requests
D7
Data Bus
D0
Request Acknowledge and Special Signals
BUSAK
RFSH
HALT
M1
MREQ
IORQ
RD
WR
Control Signals

Digital circuit pins

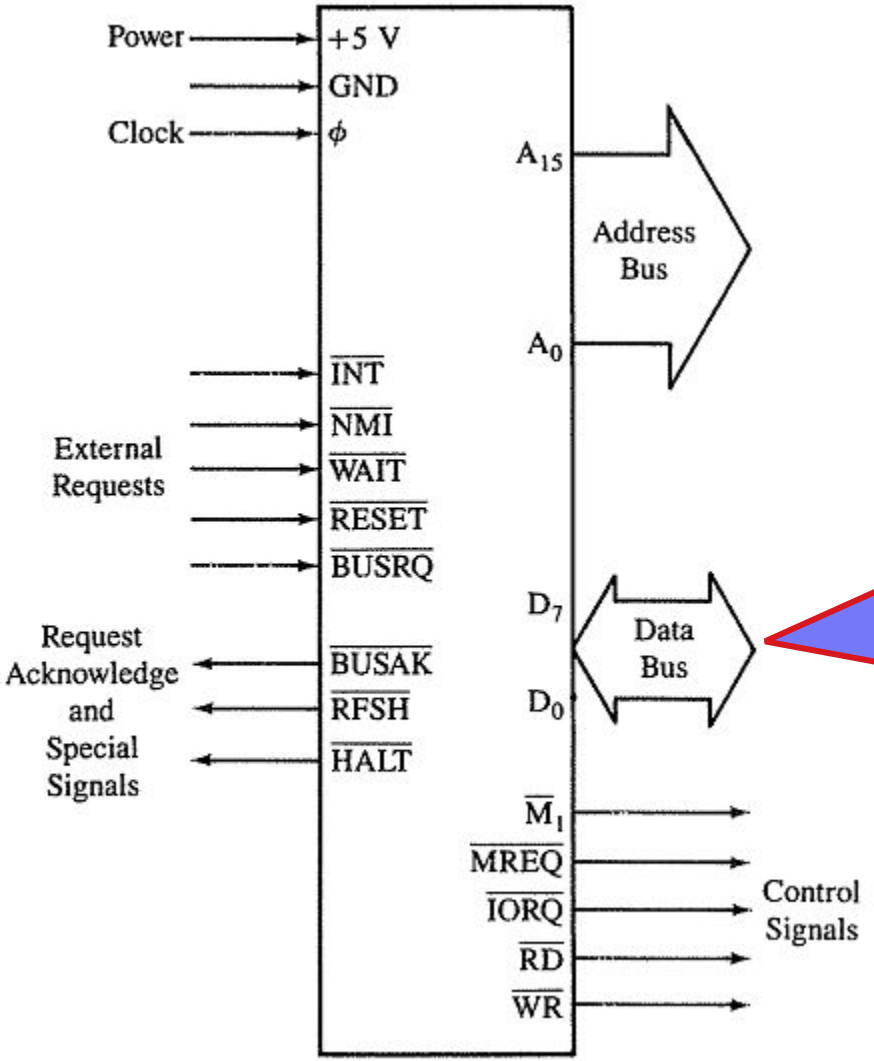
- Pins in terms of signal direction
  - Input
  - Output
  - Input/Output
- Possible status of an output pin
  - Logical zero (0V)
  - Logical one (+5V)
  - Hi-z (high impedance for tri-state pins)
- Signals in terms of activation level
  - Active-high (1 means active)
  - Active-low (0 means active)

Z80 Pin descriptions



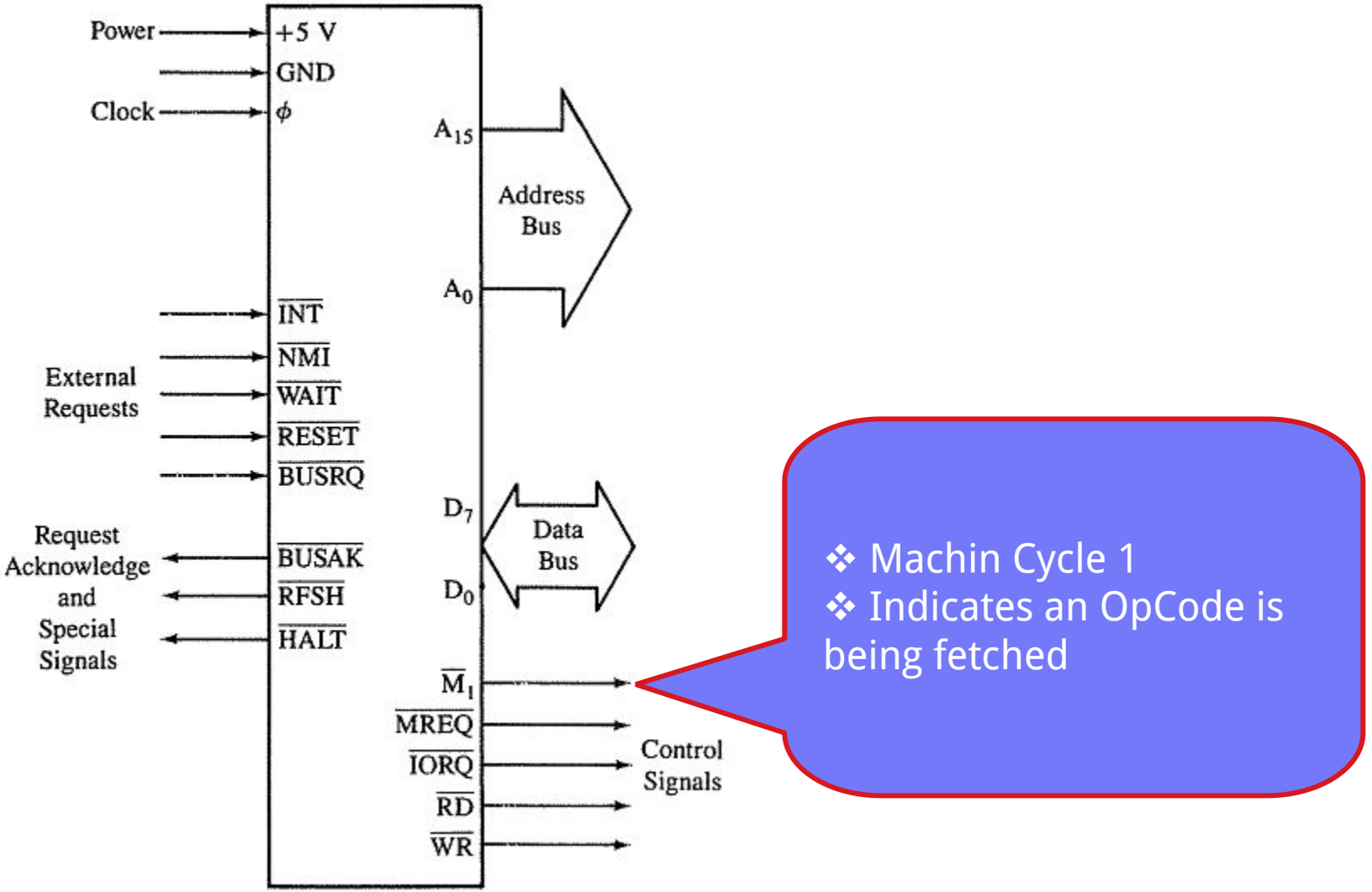
- 16 unidirectional tri-state lines
- Capable of addressing up to 64K memory locations
- Is used to address memories and I/O devices

Z80 Pin descriptions

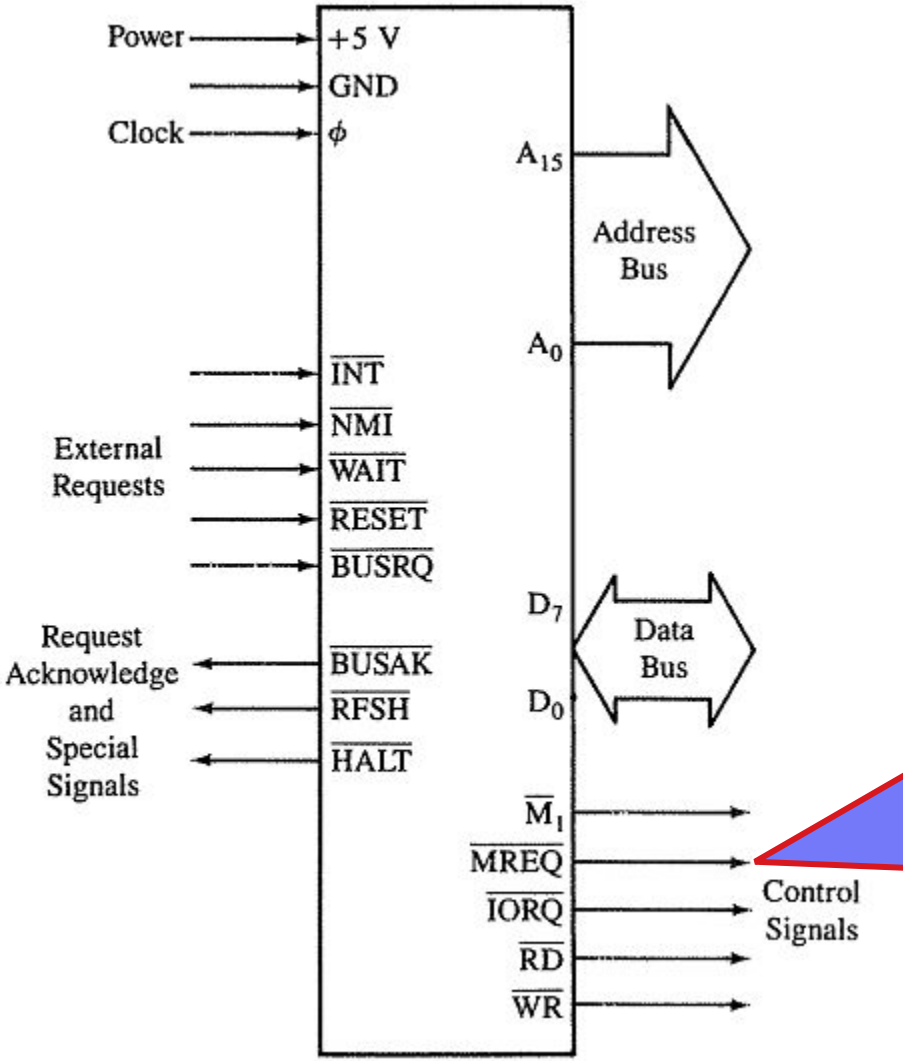


- 8 bidirectional tri-state lines
- Used to flow date between microprocessor and memories or I/O devices

Z80 Pin descriptions

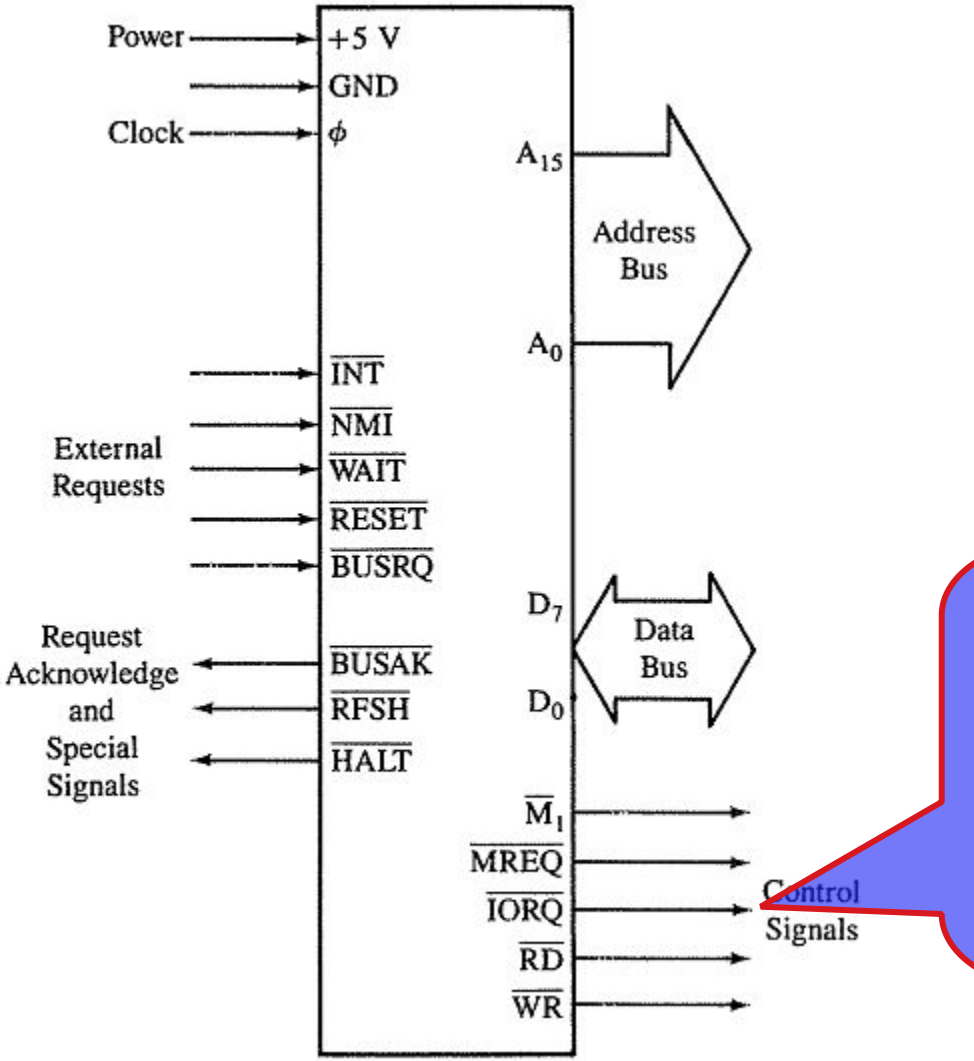


Z80 Pin descriptions



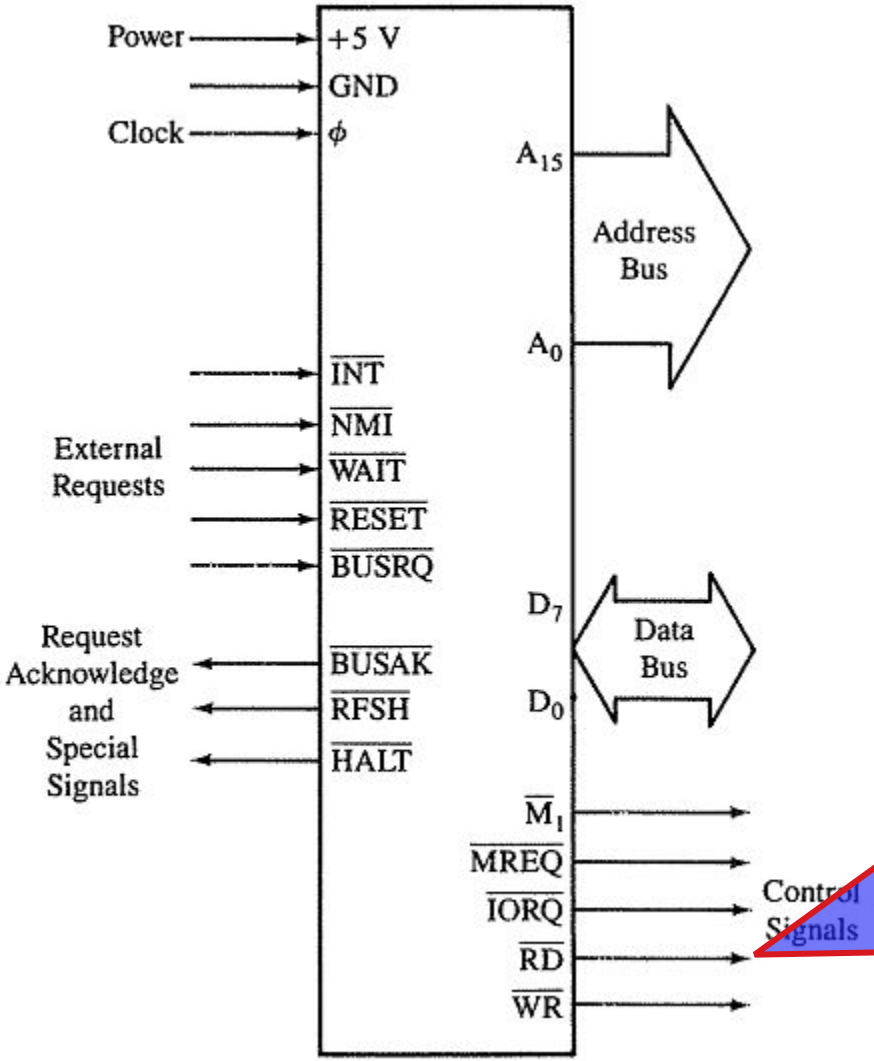
- Memory request
- Tri-state active-low
- Indicates that the address bus holds a valid address for a memory operation to be done

Z80 Pin descriptions



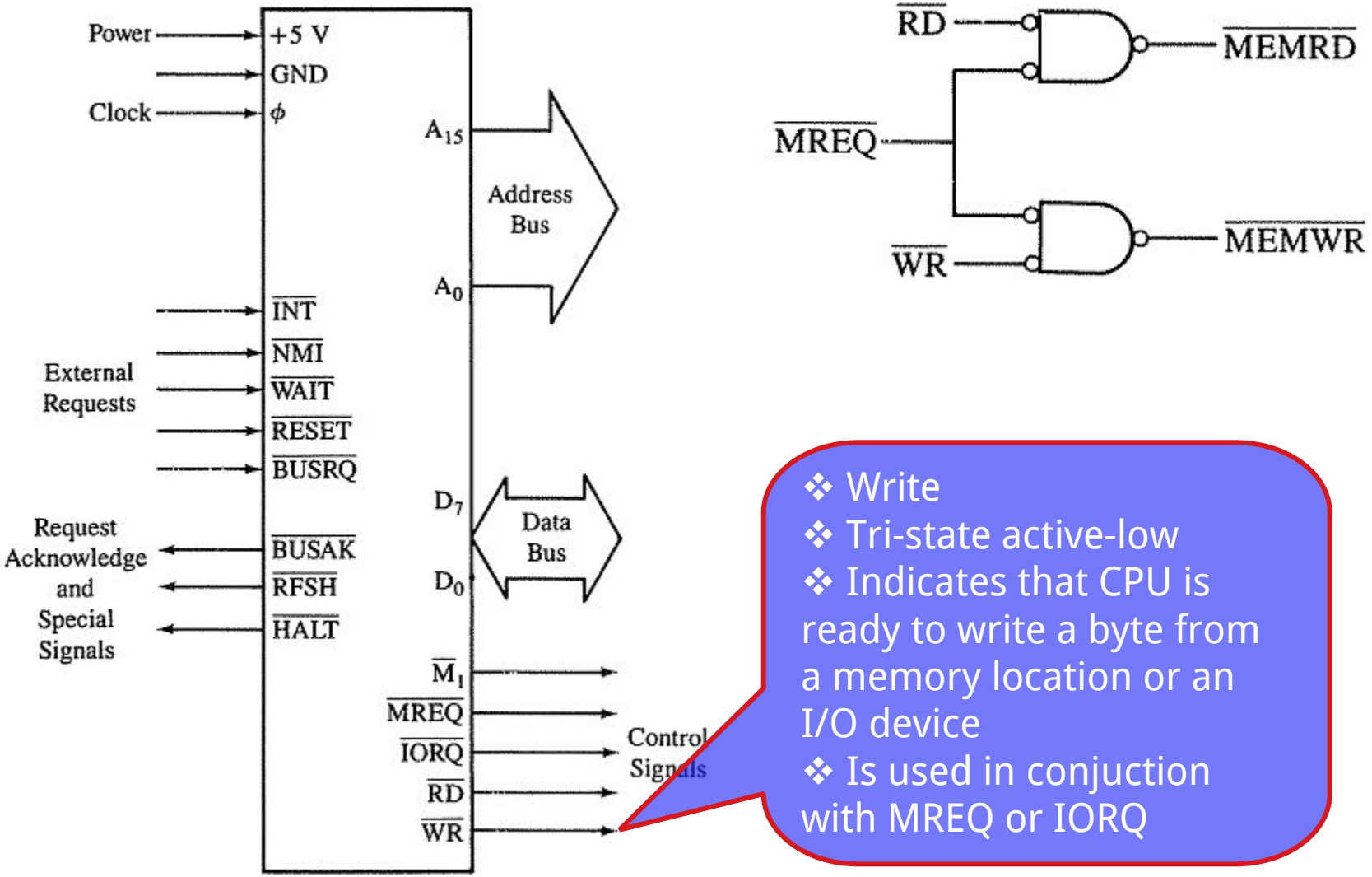
- Input/Output request
- Tri-state active-low
- Indicates that the address bus holds a valid address for an IO operation to be done

Z80 Pin descriptions



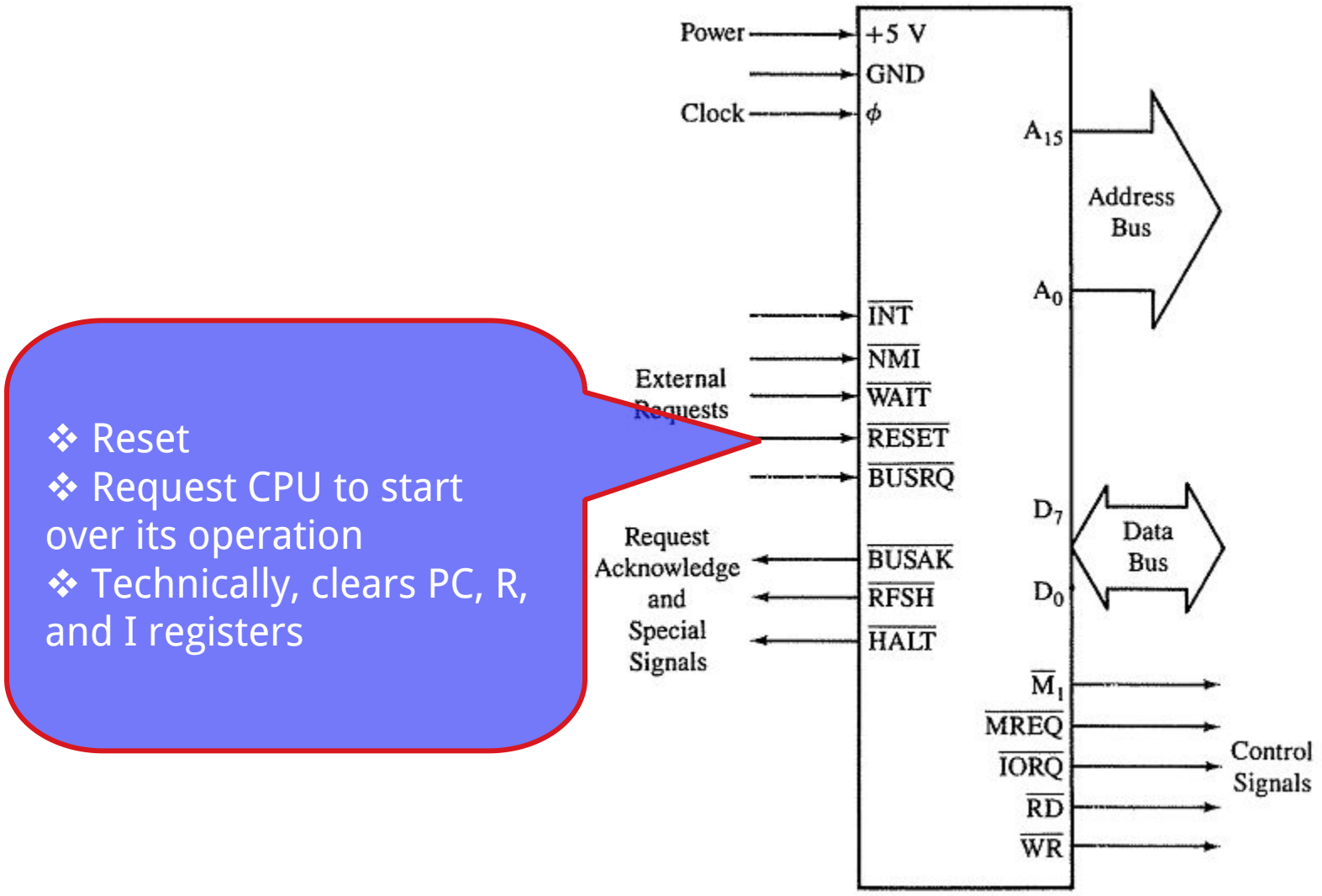
- Read
- Tri-state active-low
- Indicates that CPU is ready to read a byte from a memory location or an I/O device
- Is used in conjuction with MREQ or IORQ

Z80 Z80 Pinout



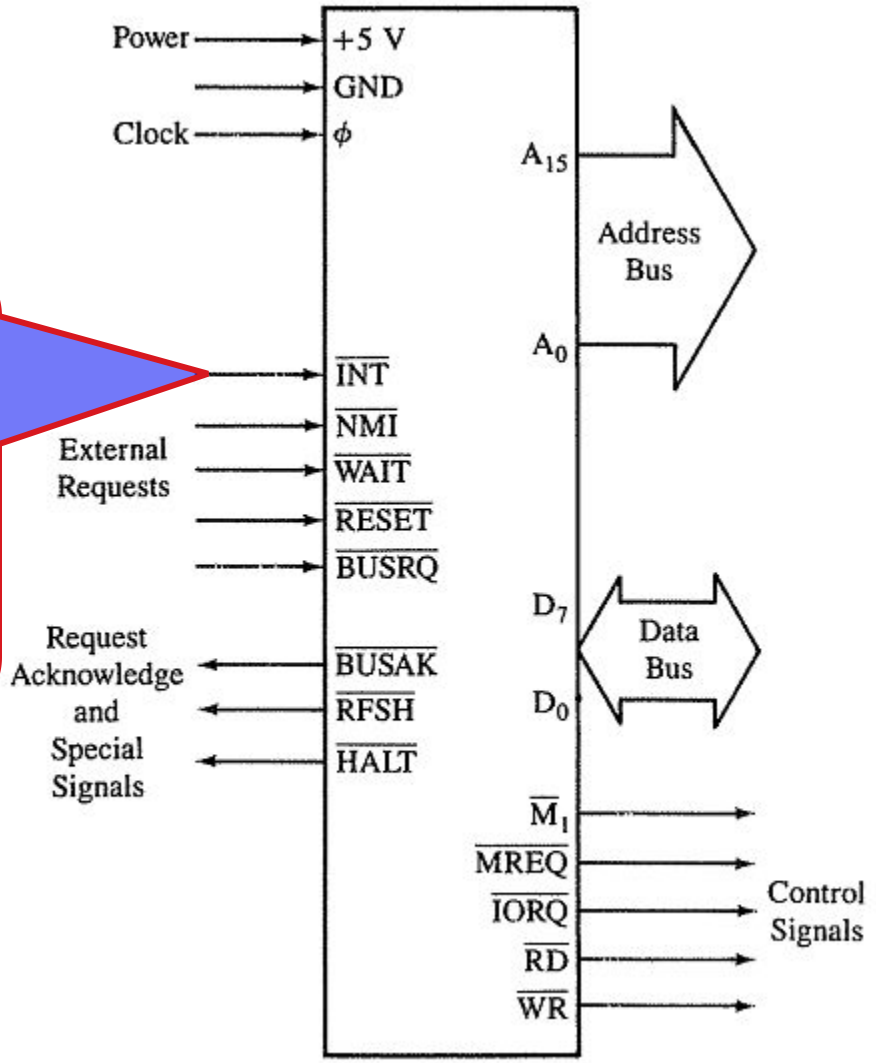
- Write
- Tri-state active-low
- Indicates that CPU is ready to write a byte from a memory location or an I/O device
- Is used in conjuction with MREQ or IORQ

Z80 Pin descriptions



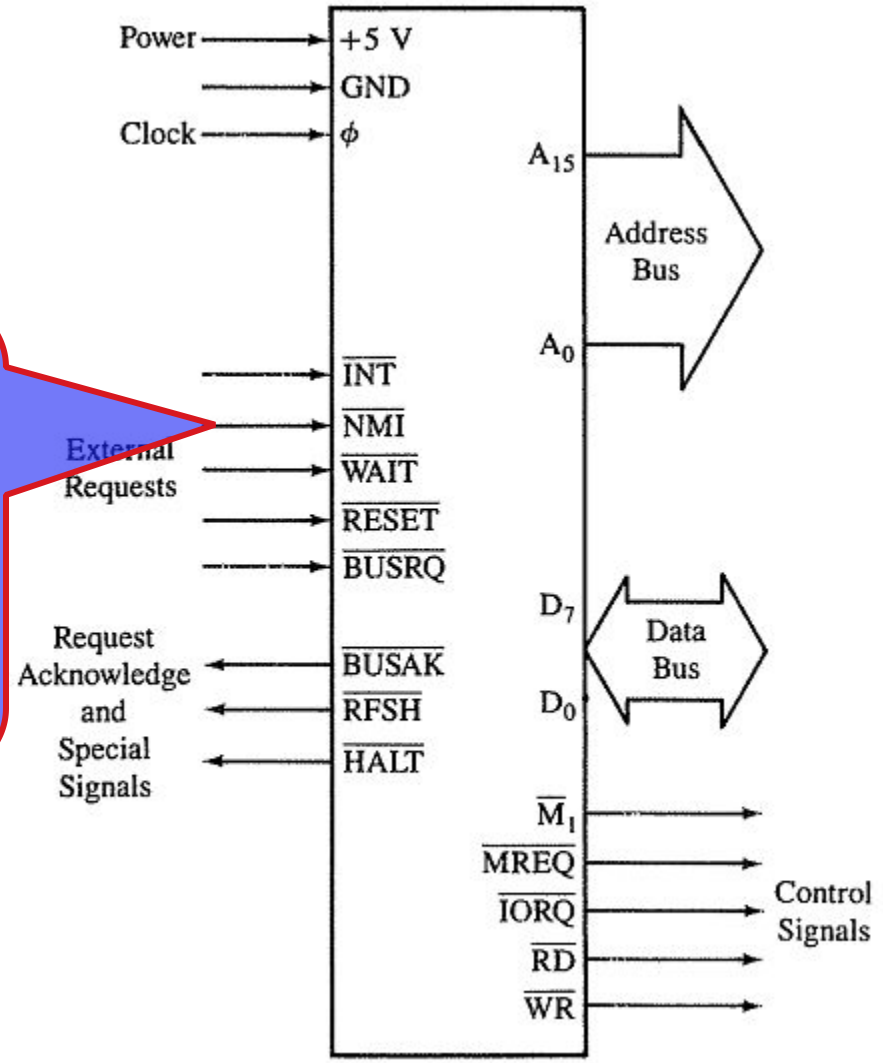
Z80 Pin descriptions

- Interrupt request
- Initiated by I/O device to interrupt the microprocessor operation
- This interrupt request is maskable

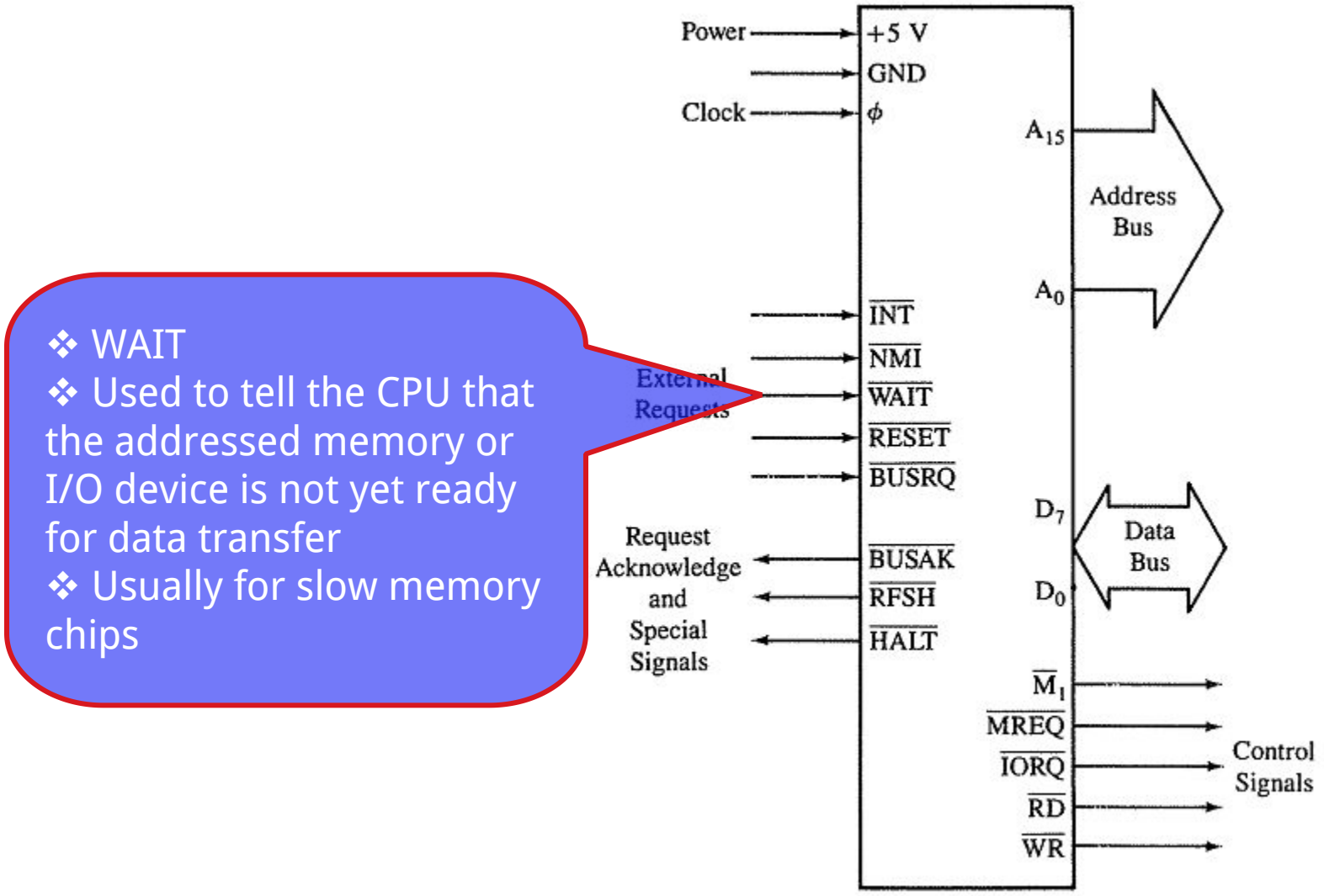


Z80 Pin descriptions

- ❖ Nonmaskable Interrupt request
- ❖ Initiated by I/O device to interrupt the microprocessor operation
- ❖ Usually used to implement emergency mechanisms

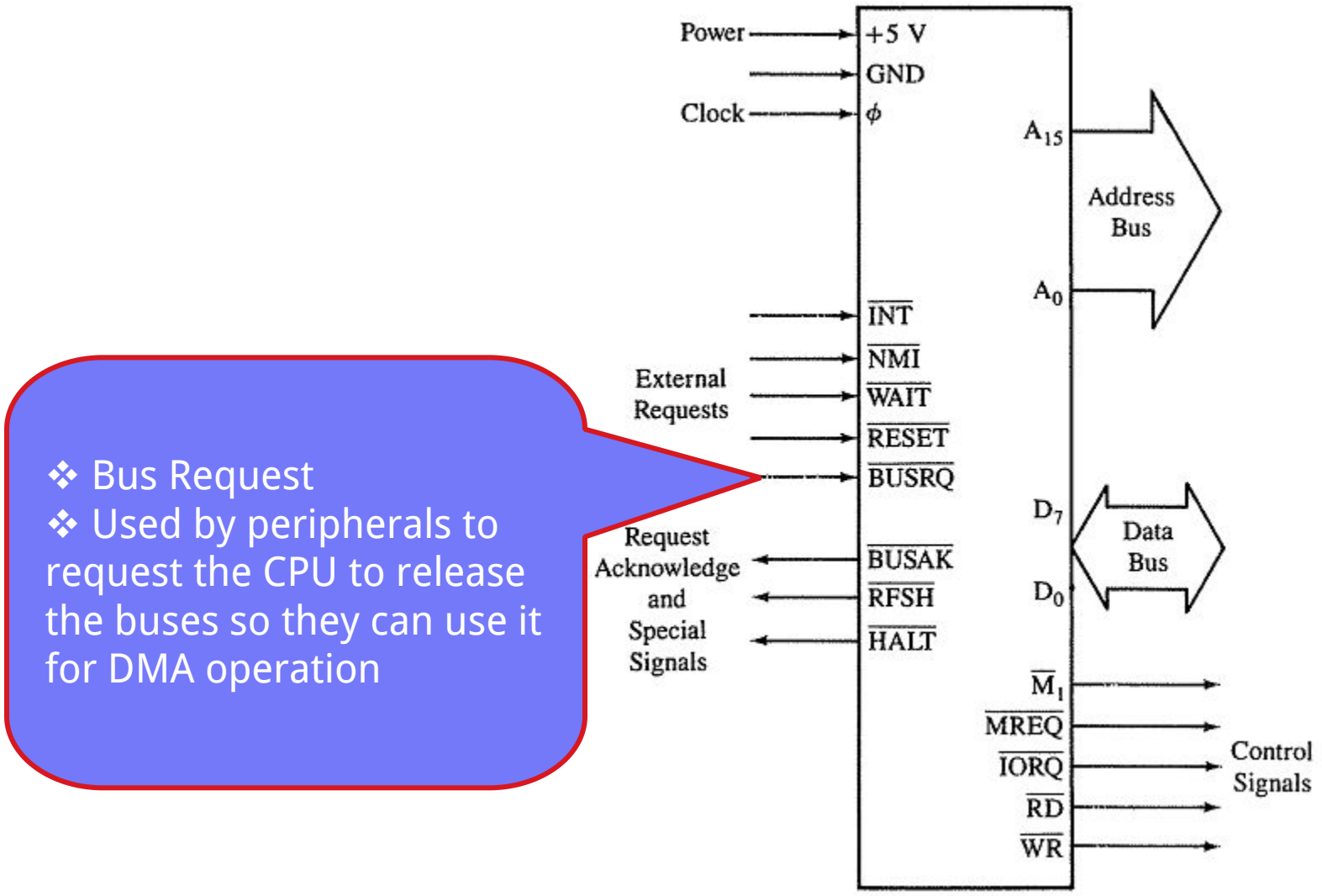


Z80 Pin descriptions

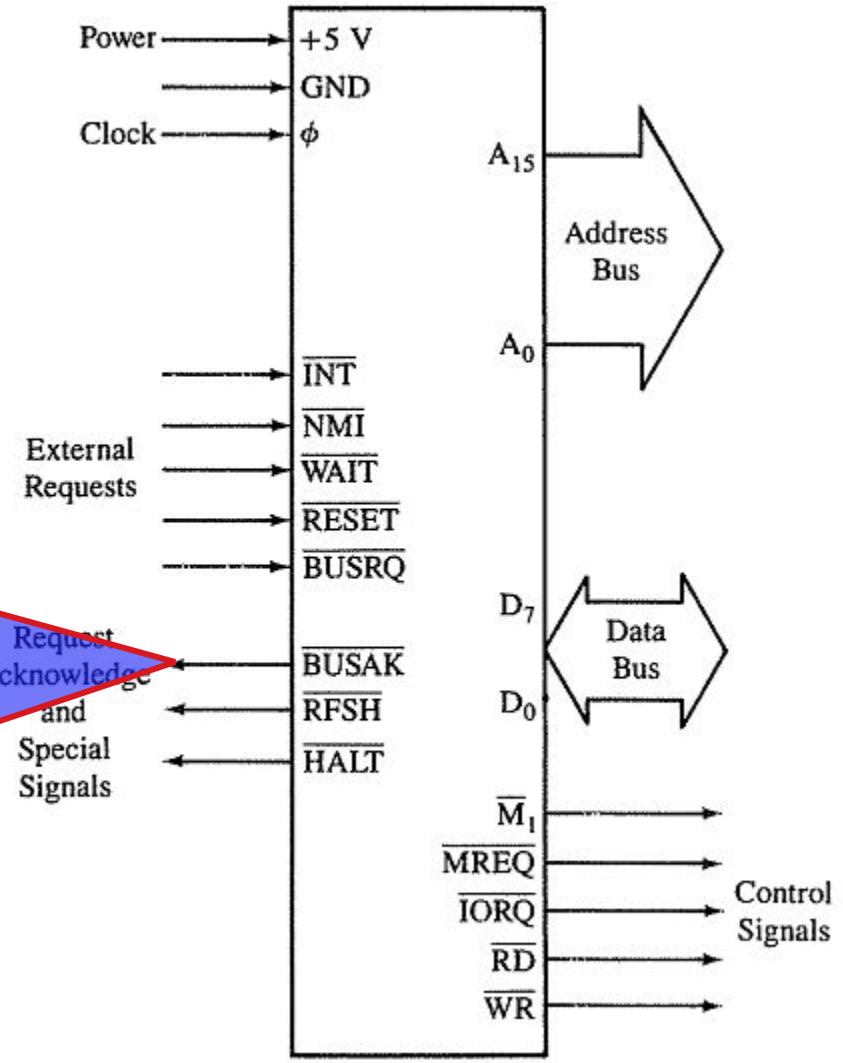


- WAIT
- Used to tell the CPU that the addressed memory or I/O device is not yet ready for data transfer
- Usually for slow memory chips

Z80 Pin descriptions

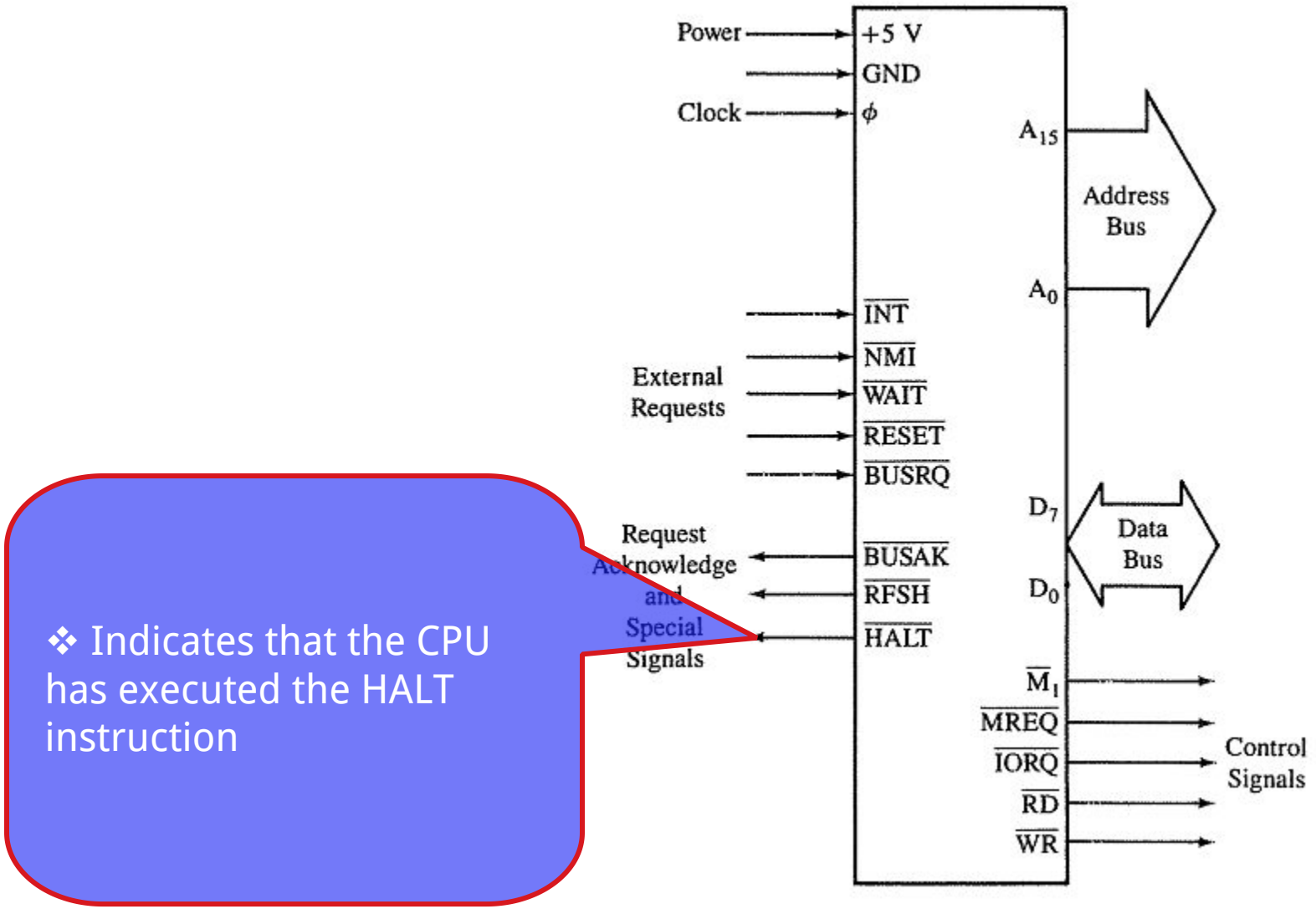


Z80 Pin descriptions



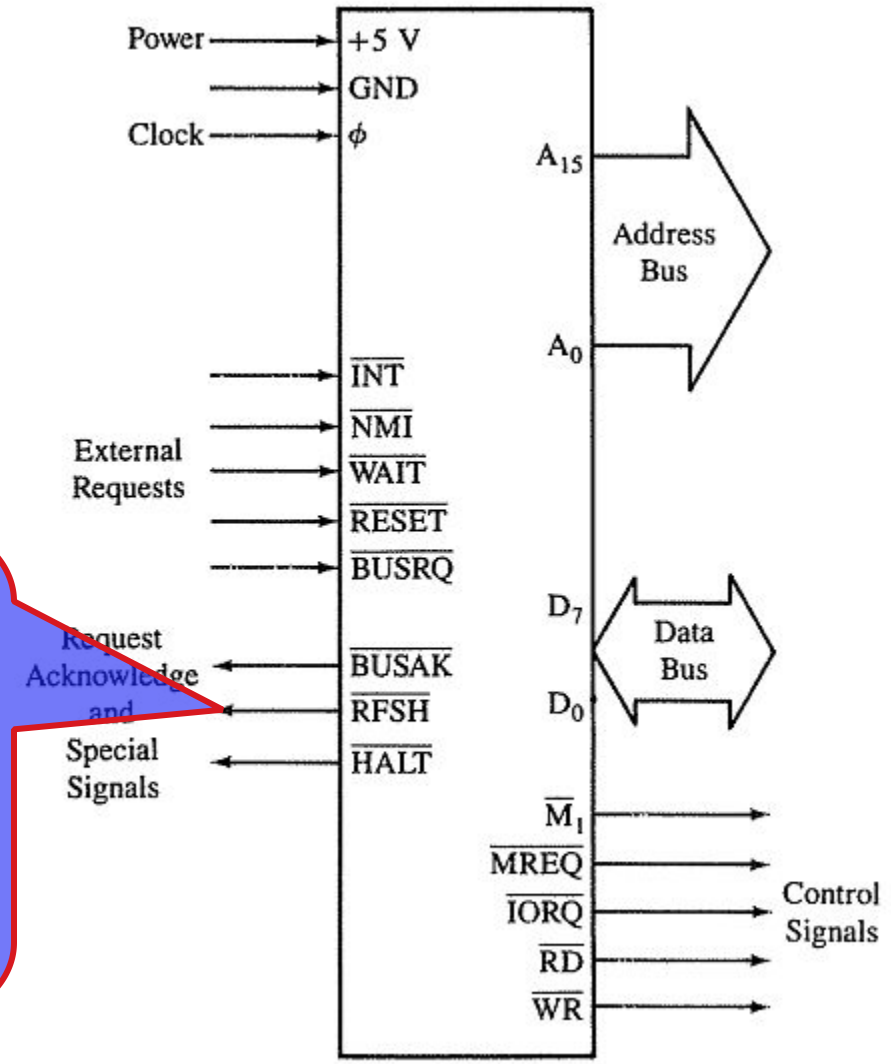
- Bus acknowledge
- In response to BUSRQ
- Tells the external device that buses are in high-impedance state by CPU and can be used by the external device

Z80 Pin descriptions



❖ Indicates that the CPU has executed the HALT instruction

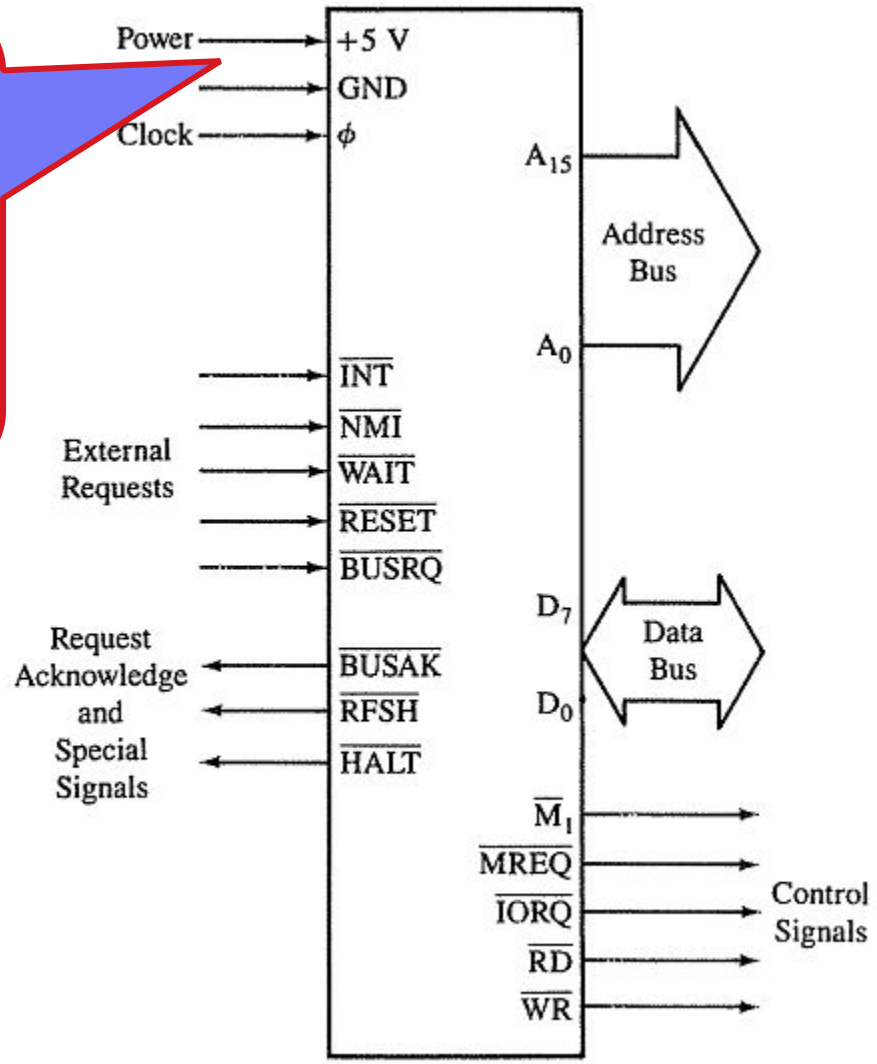
Z80 Pin descriptions



- Used for refreshing the content of dynamic memories
- Indicates that A6-A0 hold the refresh address

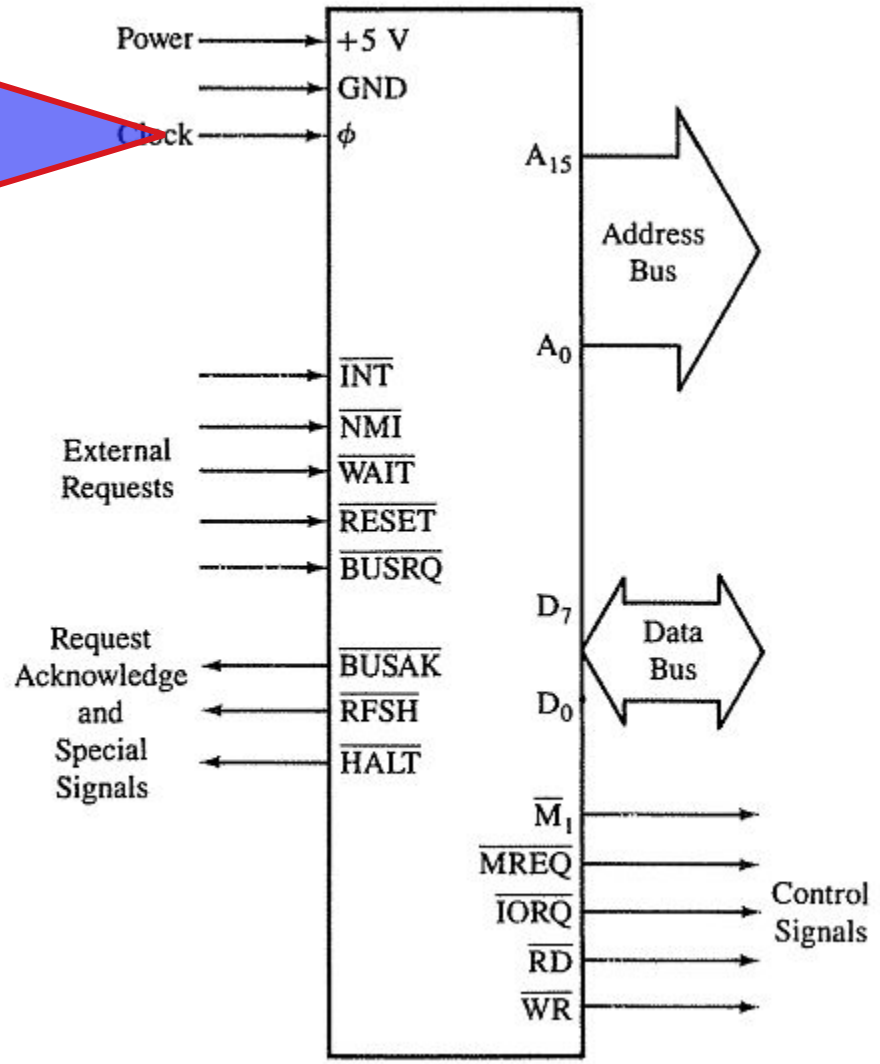
Z80 Pin descriptions

❖ (+5V, GND) Power supply source

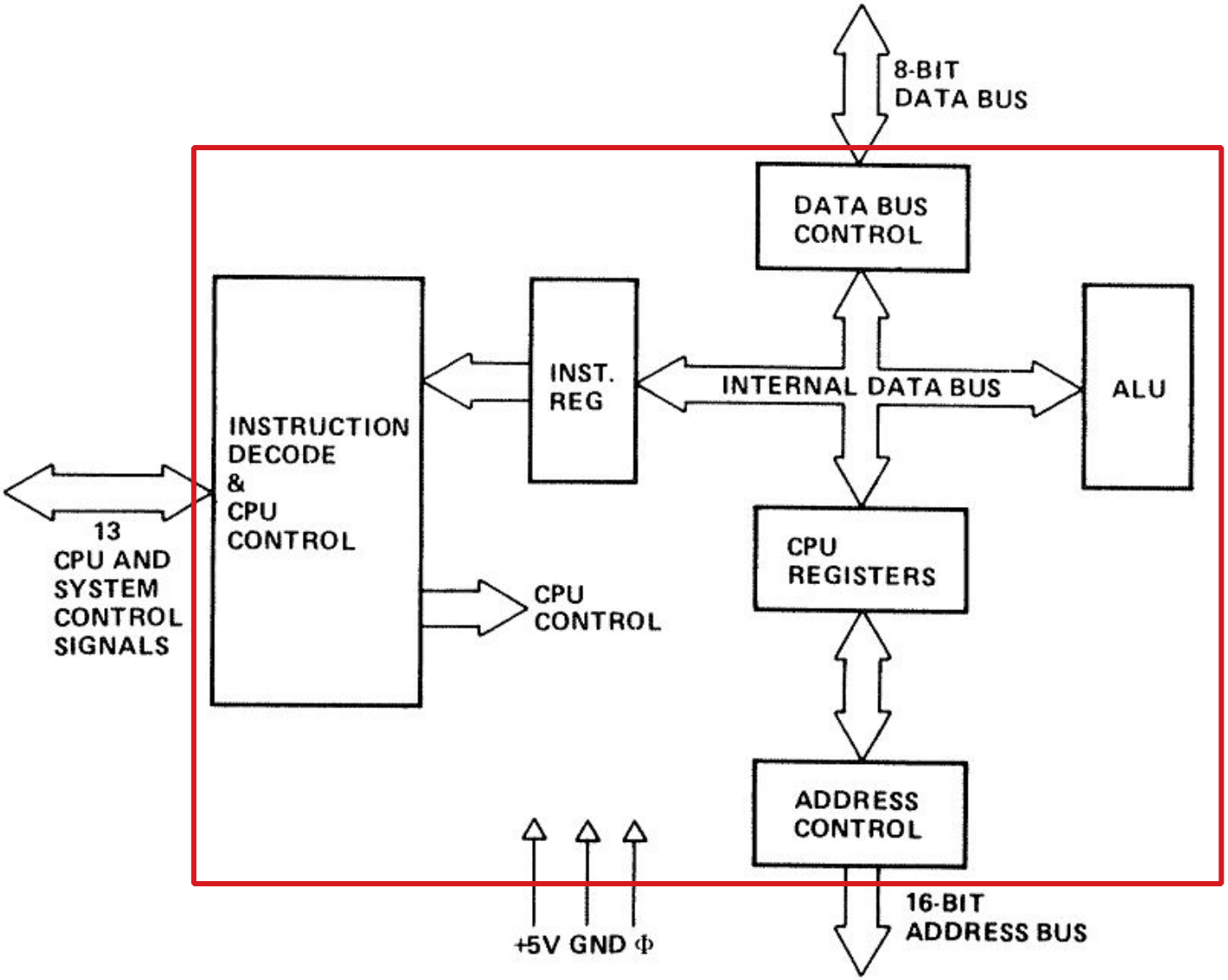


Z80 Pin descriptions

- Single phase clock source
- Z80 needs external clock circuitry (oscillator)
- With some other processors we can connect a crystal directly to the chip

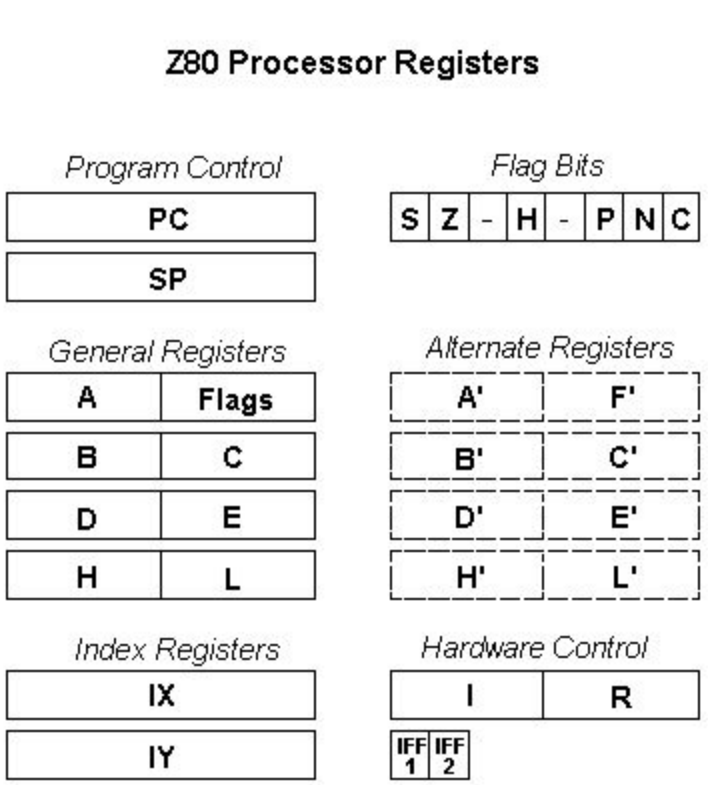


Z80 Internal block diagram



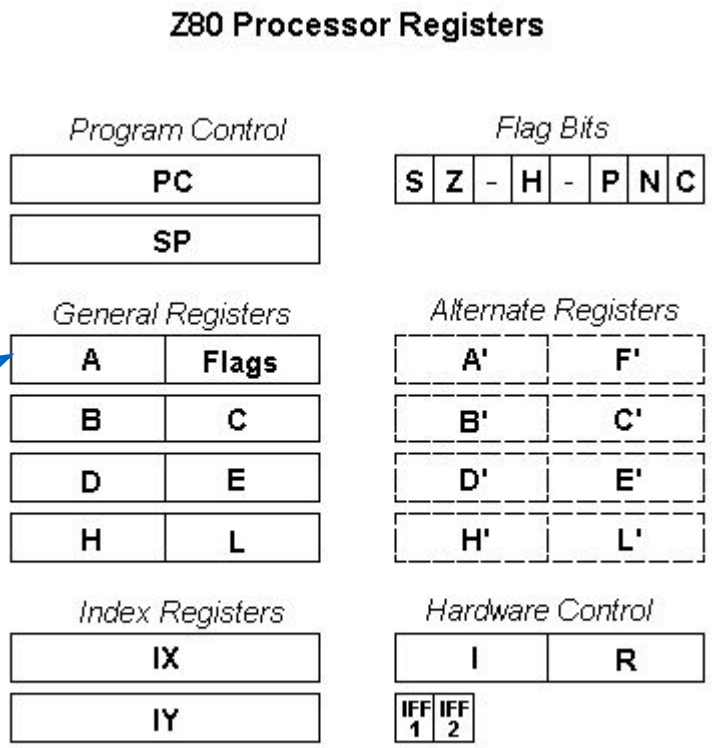
Z80 programming model

- Internal registers and flags



Z80 registers

- Accumulator
- Stores 8-bit data
- The first operand of arithmetic and logical instructions
- Stores the result of arithmetic and logical instructions



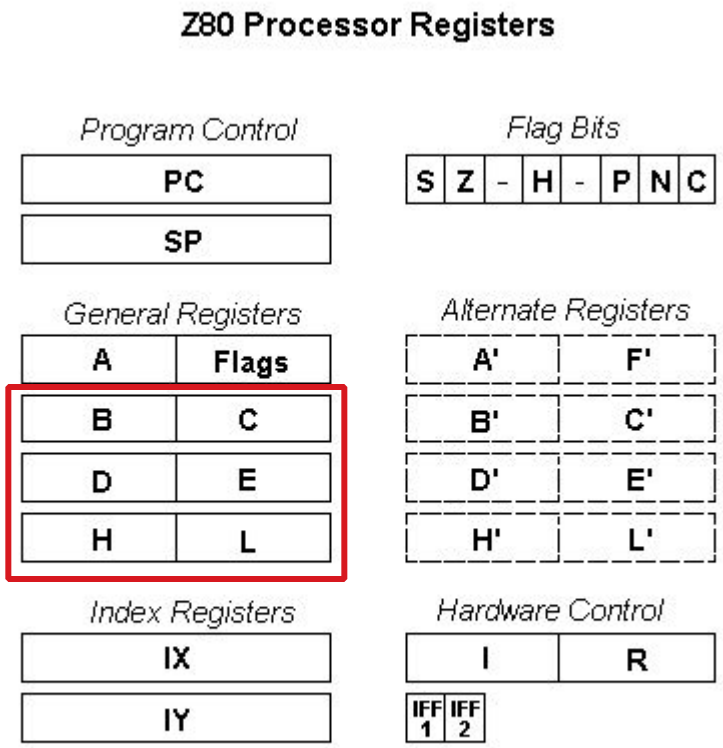

```
; A ← A + 12H
ADD     A, 12H
```

Z80 registers

- General-purpose registers
- Each one is 8 bits wide
- Can be used as 16-bit pairs BC, DE, and HL for 16 bit operations or holding memory addresses

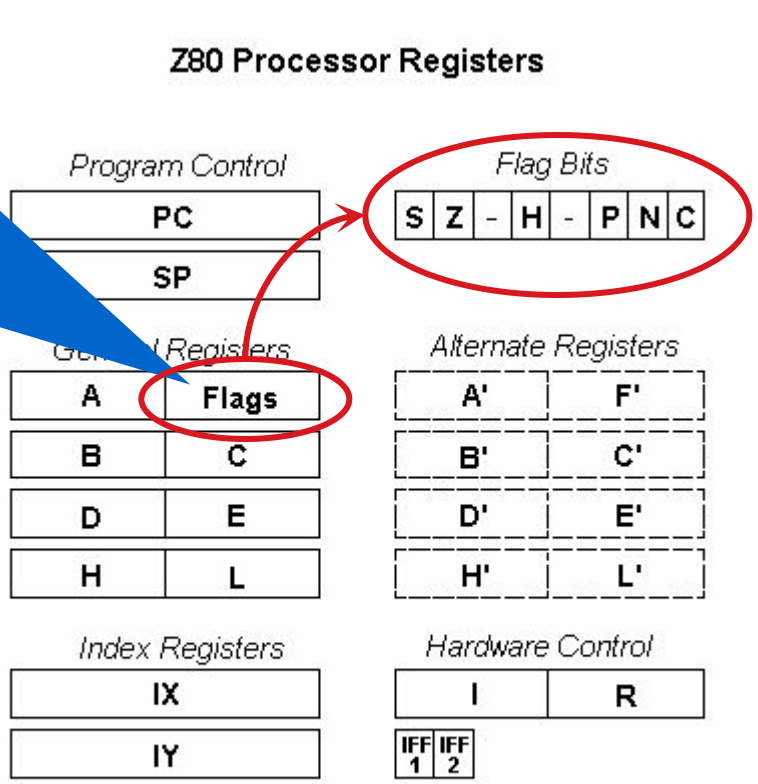
```
; A ← A+B
ADD     A, B

; A ← MEM[HL]
LD      A, (HL)
```



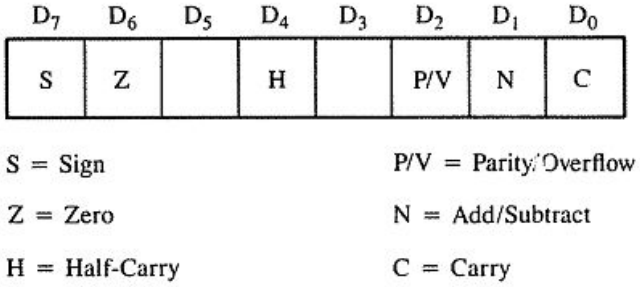
Z80 registers

- Flags registers
- Are set after each ALU operation
- Can be examined in the program if necessary
- Make conditional jumps and calls possible



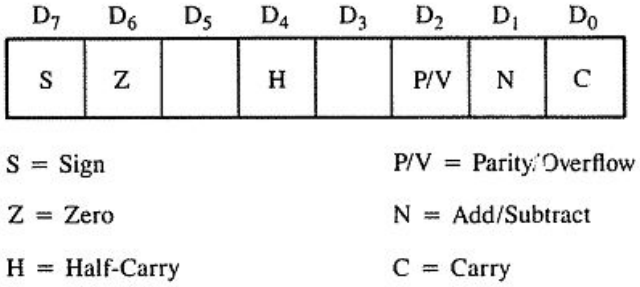

```
; Jump to 2050H if
; C flag is set
JP      C, 2050H
```

Flag bits



- Flag bits
  - C – Carry flag
    - Is set when an addition generates a carry or a subtraction generates a borrow
    - May be set by the result of shift instructions
    - May be set or reset programmatically by SCF and CCF instructions
  - Z – Zero flag
    - Is set when the result of an 8-bit operation is zero
    - Is also affected by the result of comparisons and bit tests
    - Is also affected by some other instructions
  - S – Sign flag
    - Is set when the most significant bit of the ALU operation result is 1
    - Means negative result when operands are interpreted as signed numbers
    - Is also affected by some other instructions

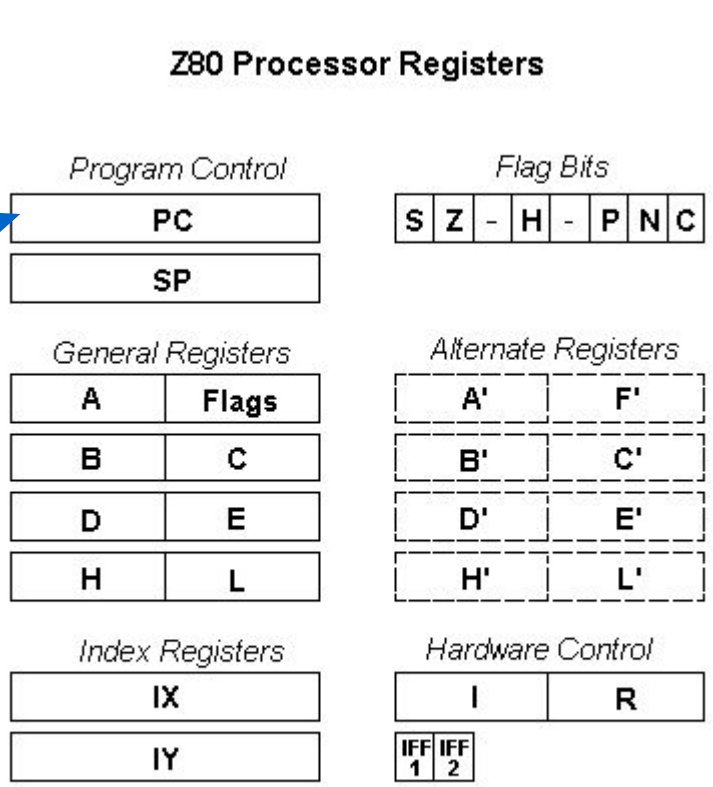
Flag bits



- Flag bits
  - P/V – Parity/Overflow flag
    - Parity of the result of logical instructions (1 if the number of 1's is even)
    - Overflow of the result of arithmetic signed instructions
    - Is also affected by some other instructions
  - H – BCD half-carry flag
    - BCD carry or borrow between bit 3 and bit 4
    - Used internally for BCD operations
    - Can not be tested by conditional jumps
  - N – BCD subtraction
    - 1 means subtraction and 0 means addition
    - Used internally for BCD operations (to decide whether add 6 or subtract 6 for correcting result)
    - Can not be tested by conditional jumps

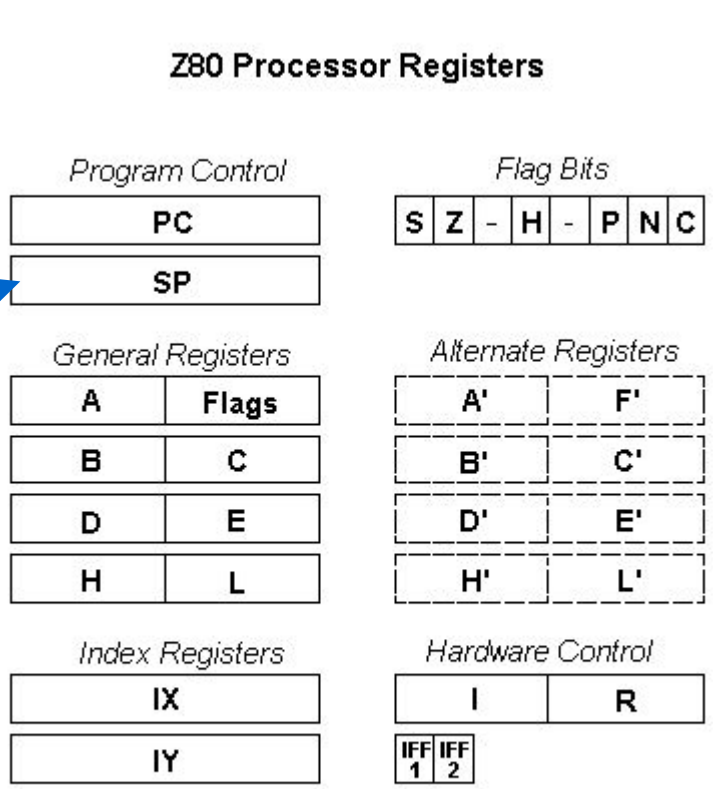
Z80 registers

- Program counter
- Points to the memory address from which the next instruction is to be fetched
- Programmer can only perform load-store operations on PC, not arithmetic nor logical instructions



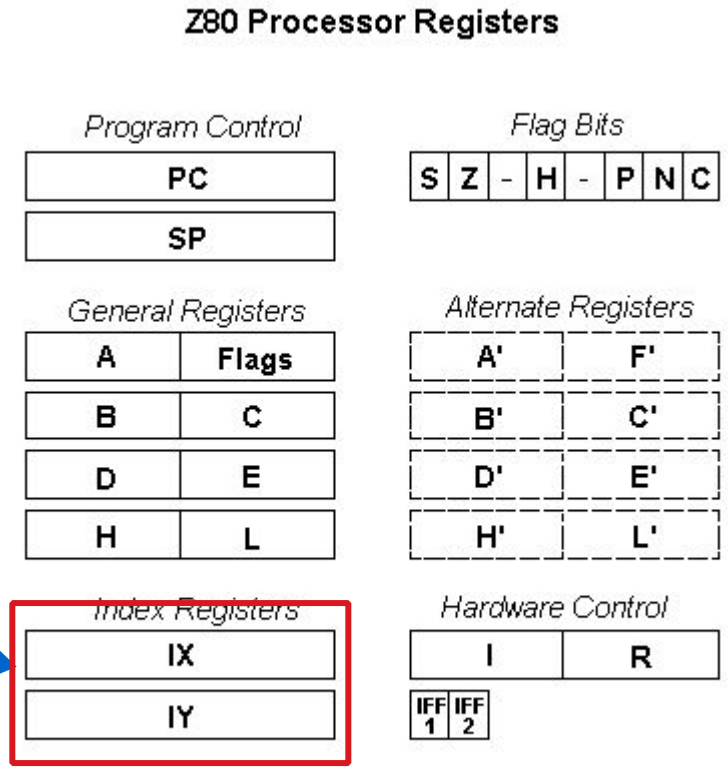
Z80 registers

- Points to the top of stack in the memory
- Is decremented when data is pushed into stack
- Is incremented when data is popped
- Stack is important for storing return address of subroutines



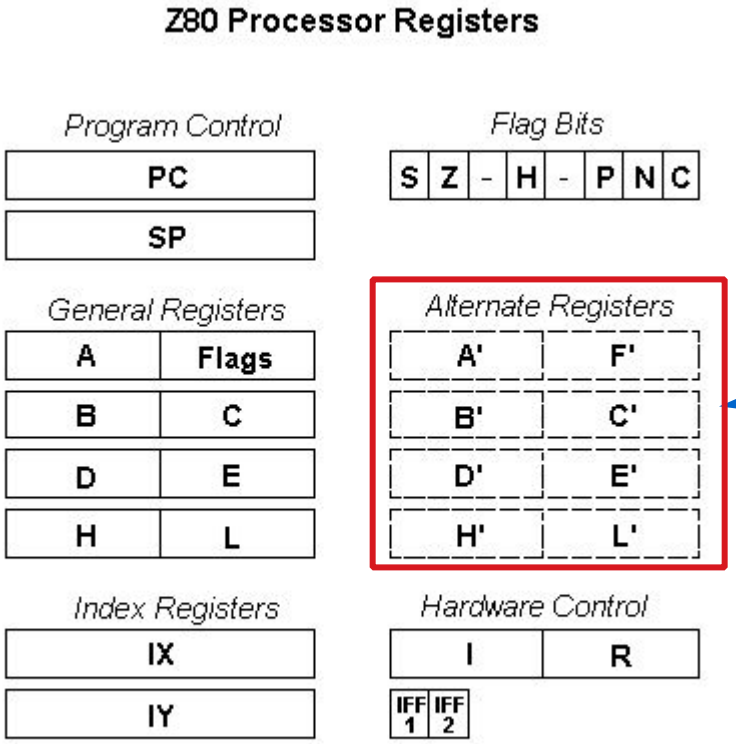
Z80 registers

```
; MEM[IX+5] ← 12H
LD      (IX+5), 12H
```



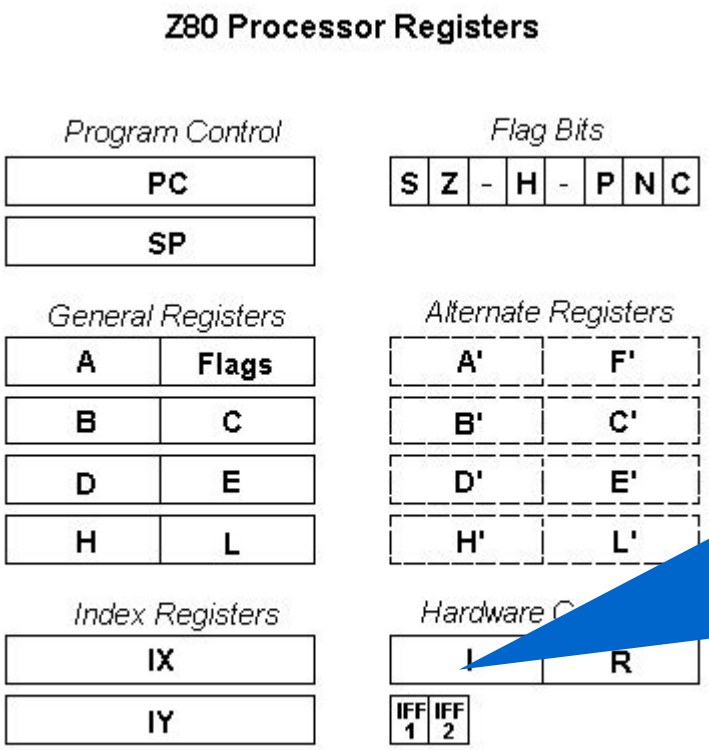
- Index registers
- Used for indexed memory addressing
- Accept displacement (Unlike BC, DE, HL)

Z80 registers



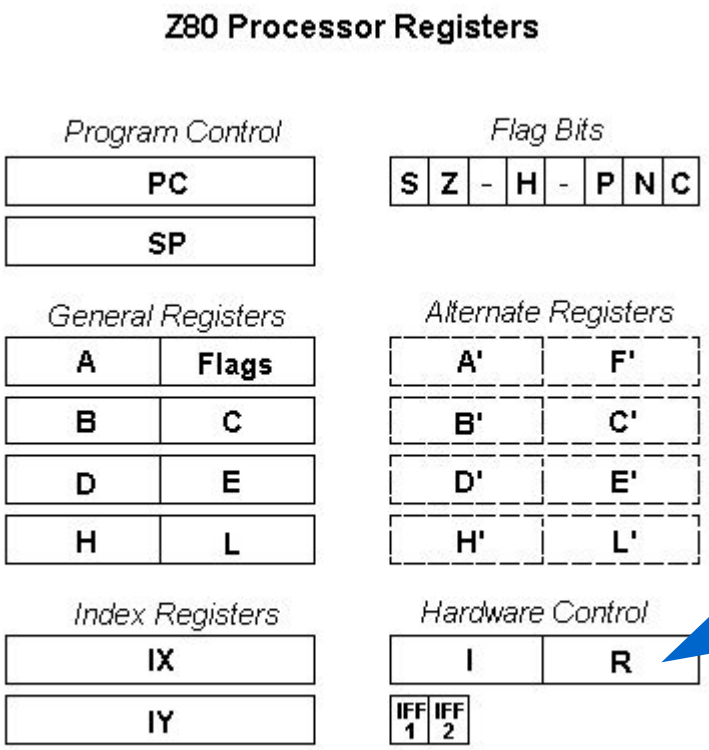
- Duplicate of general-purpose registers
- Programmer can easily switch between them
- Only one of the two sets can be used at any time
- Useful for holding environment after interrupts

Z80 registers



- Interrupt vector register
- Holds the high order 8 bits of the interrupt routine address
- The low order bits are supplied by the interrupting device
- Discussed later

Z80 registers



- Refresh register for dynamic memories
- a 7-bit counter that addresses the memory cell to be refreshed